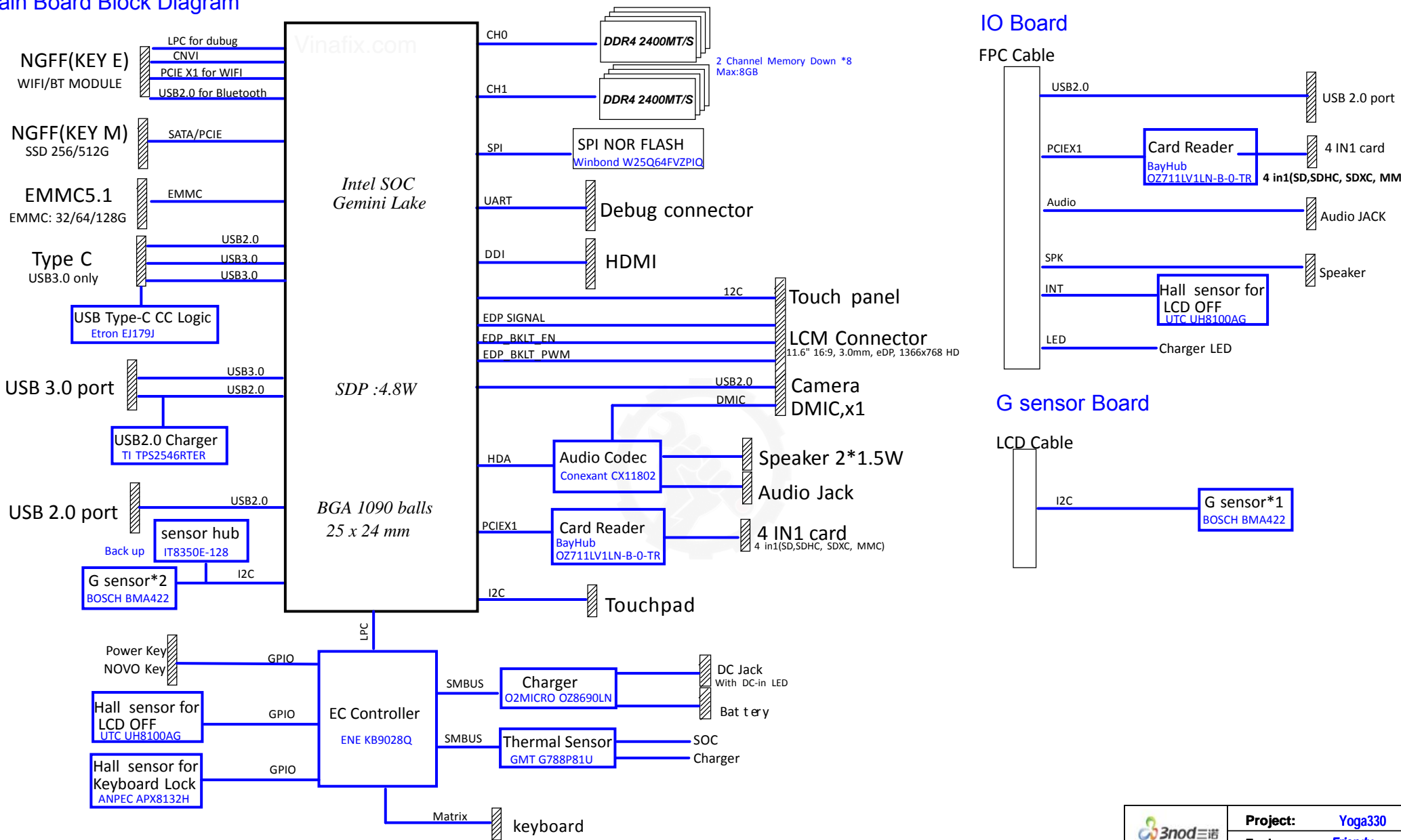
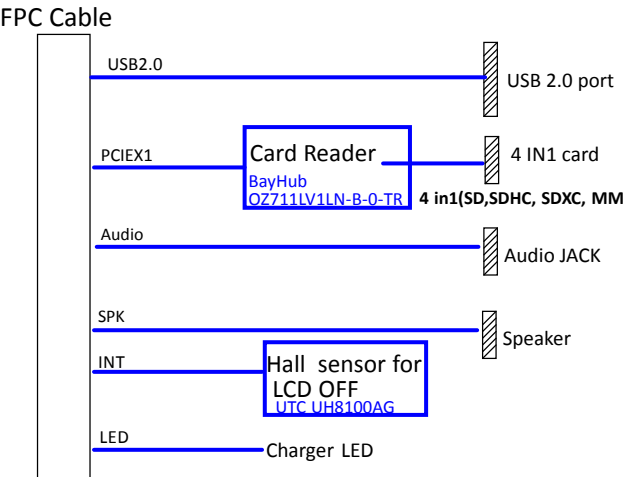


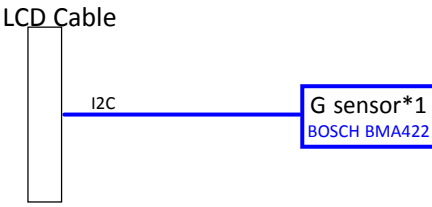
Yoga330 for Lenovo
Main Board Block Diagram



IO Board



G sensor Board



		Project: Yoga330	
		Engineer: Friendly	
Size	Title: Block Diagram	Rev	
Custom		1	V01
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27	--NC	57	--PWR-+V5P0A / +V3P3A
28	--SPI FLASH	58	--5VSX AND 3.3VSX
29	--EMMC	59	--PWR-PMIC (APW8858)
30	--SSD	60	--CHANELIST

INTERNAL ONLY

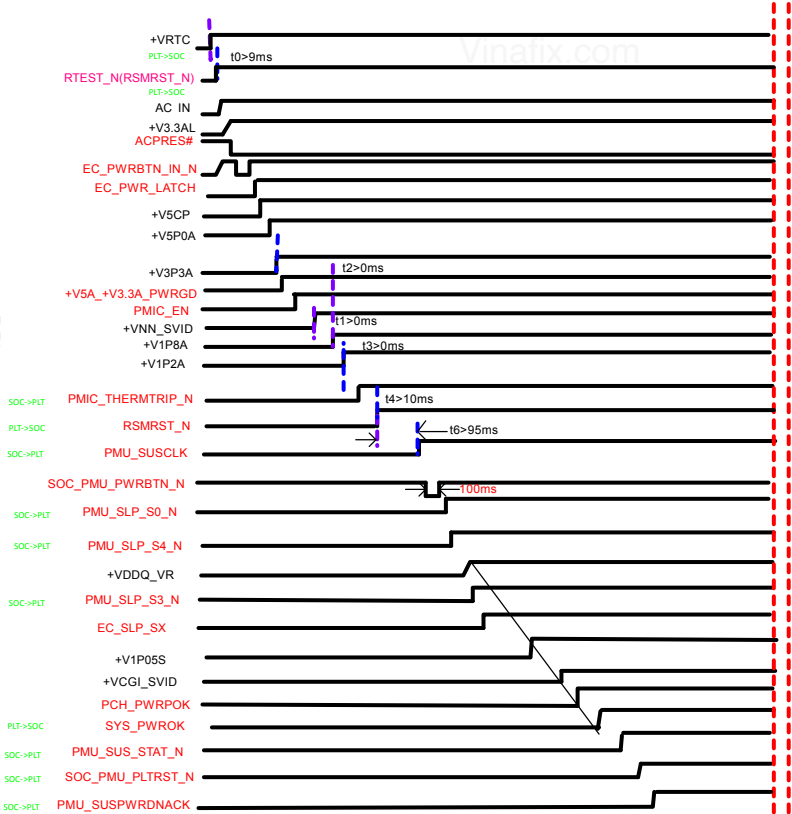
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Wed Jun 03 11:22:42 2015

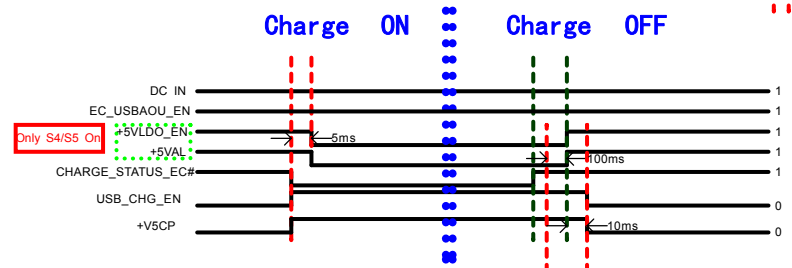
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		Engineer: Friendly	
Size	Title: Contens	Rev	
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Power sequence

G3 cold boot



G3 USB CHARGE



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shy_x_mrd_ Wed Jun 03 11:22:42 2015

		Project: Yoga330	
Size		Engineer: Friendly	
Custom		Title: Power sequence	
Date: Wednesday, November 01, 2017		Rev: V01	
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12C Map

SOC 12C Map

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I2C Port	Device	Address	Part number	Power rail
I2C0	NO use			
I2C1	NO use			
I2C2	NO use			
I2C3	Touch panel	0X20	Synaptics/S7300	P1V8A
I2C4	Touch pad	0X2C	Synaptics/TM-P3269-001	P1V8A
I2C5	Sensor/sensor hub		IT8350E-128/CX /BMA422	P3V3S
I2C6	ISH debug			
I2C7	NO use			


EC 12C Map

I2C Port	Device	Address	Part number	Power rail
SCL1/SDA1	Battery/charger	0X12	O2MICRO/OZ8690LN	P3V3A
SCL2/SDA2	Thermal sensor	0X09	GMT/G788P81U	P3V3A

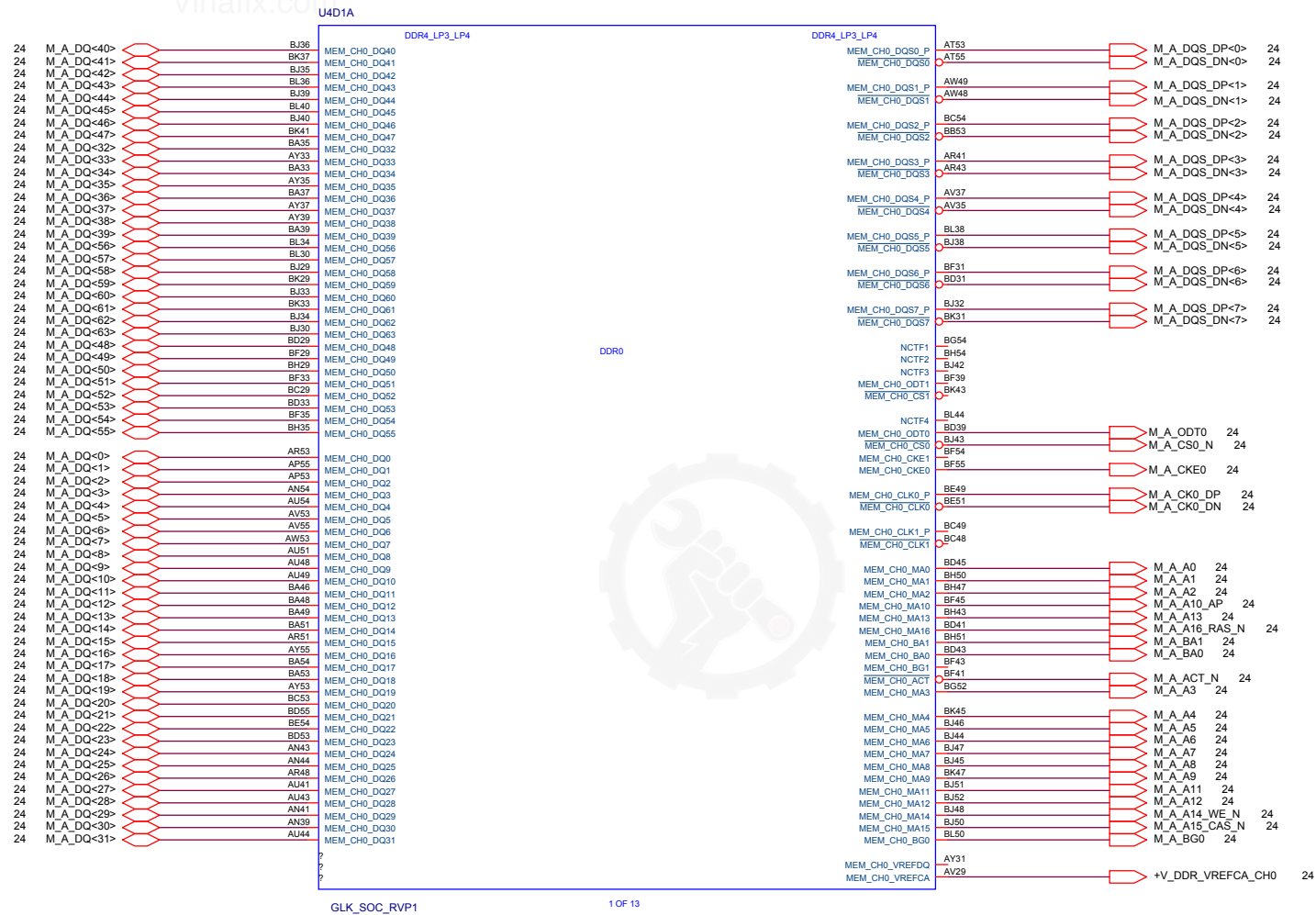
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SOC DDR4 CH0

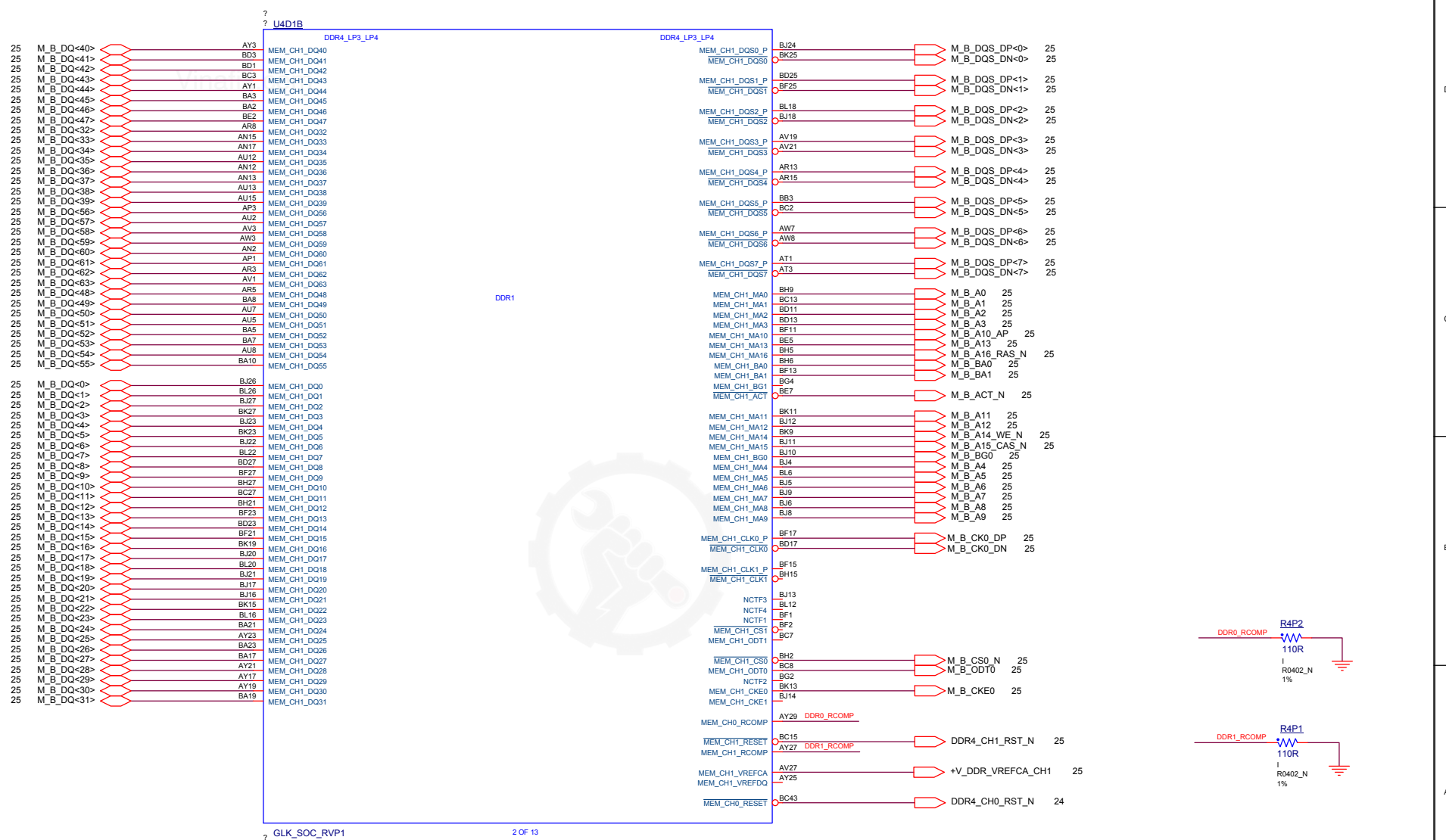


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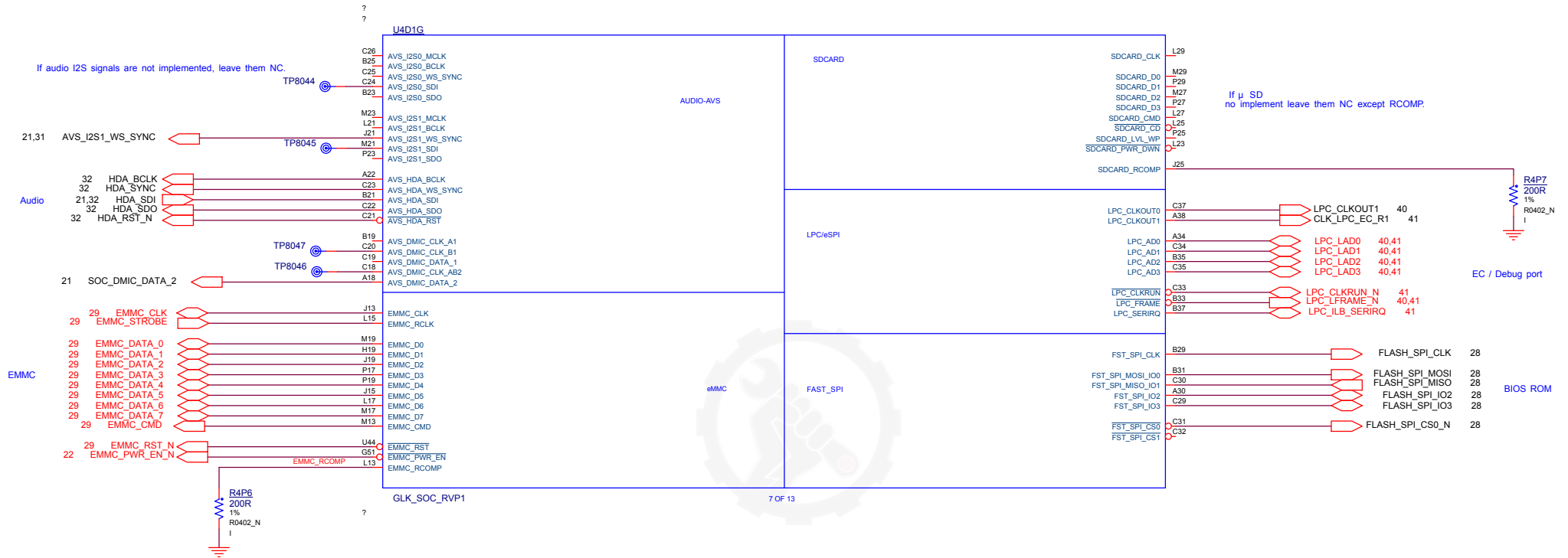
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		Engineer: Friendly	
Size	Title: SOC DDR4	Rev	
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SOC_HDA&EMMC&LPC&SPI

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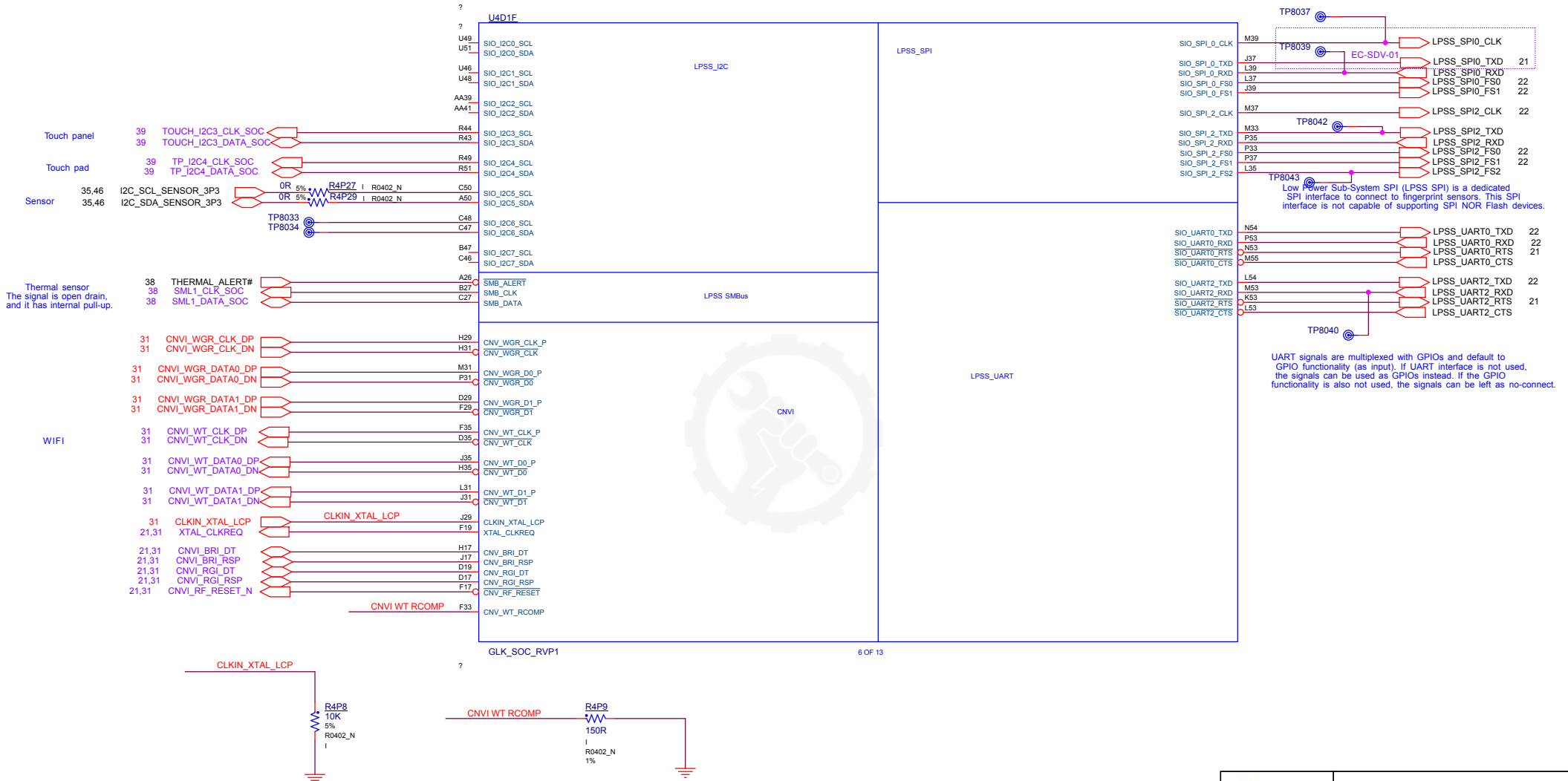
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SOC_I2C&UART

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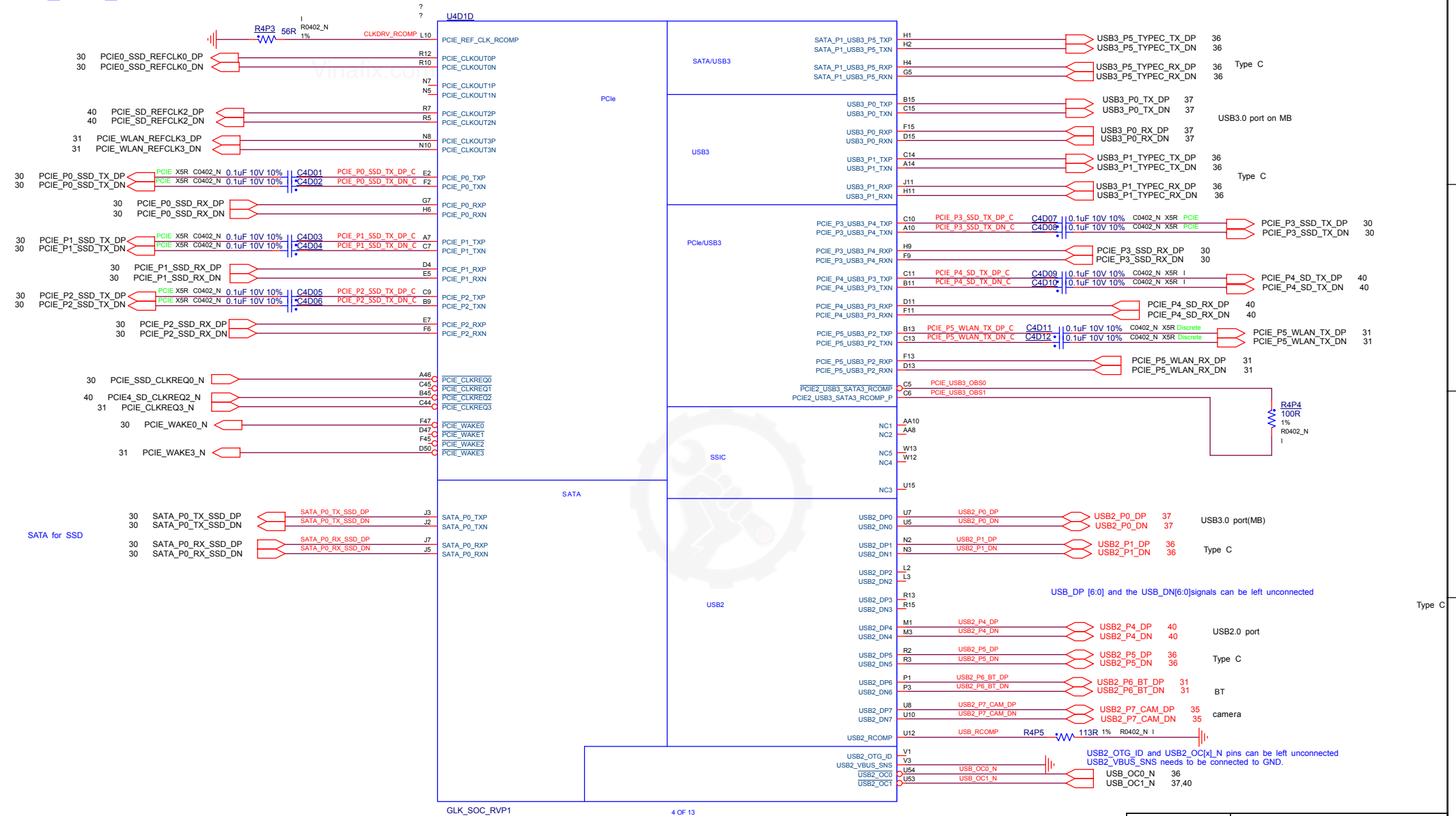


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		Engineer: Friendly		
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SOC_SOC_PCIE&SATA&USB3&USB2



GLK_SOC_RVP1

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INTERNAL ONLY

BPAGE DRAWING

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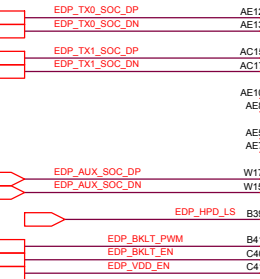
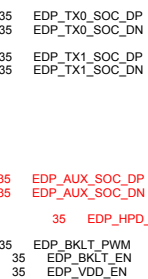
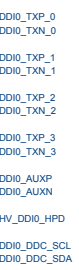
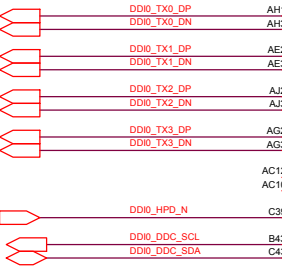
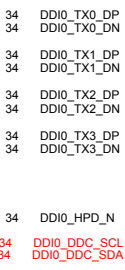
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SOC_EDP&DDI&MDSI

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U4D1C

For HDMI

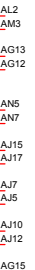


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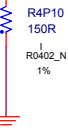
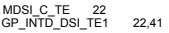
GLK_SOC_RVP1

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MDSI




If MIPI DSI is not implemented, leave them NC.



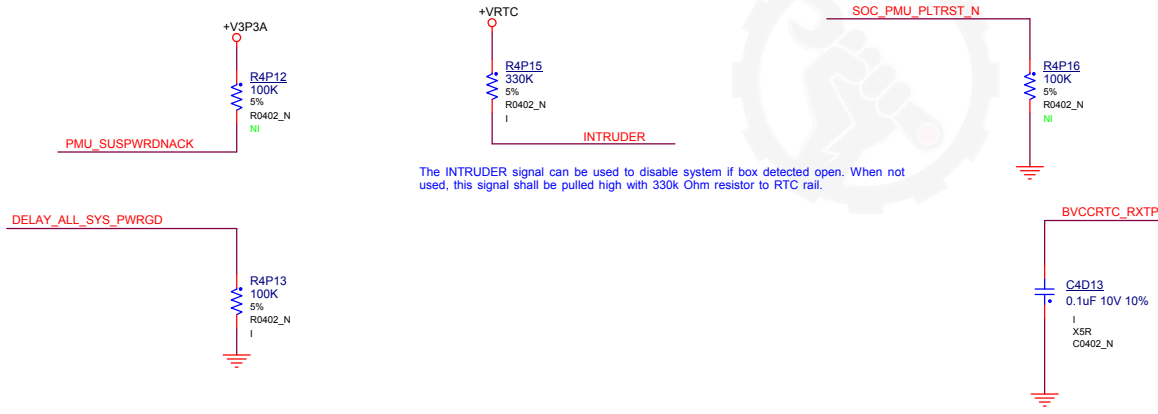
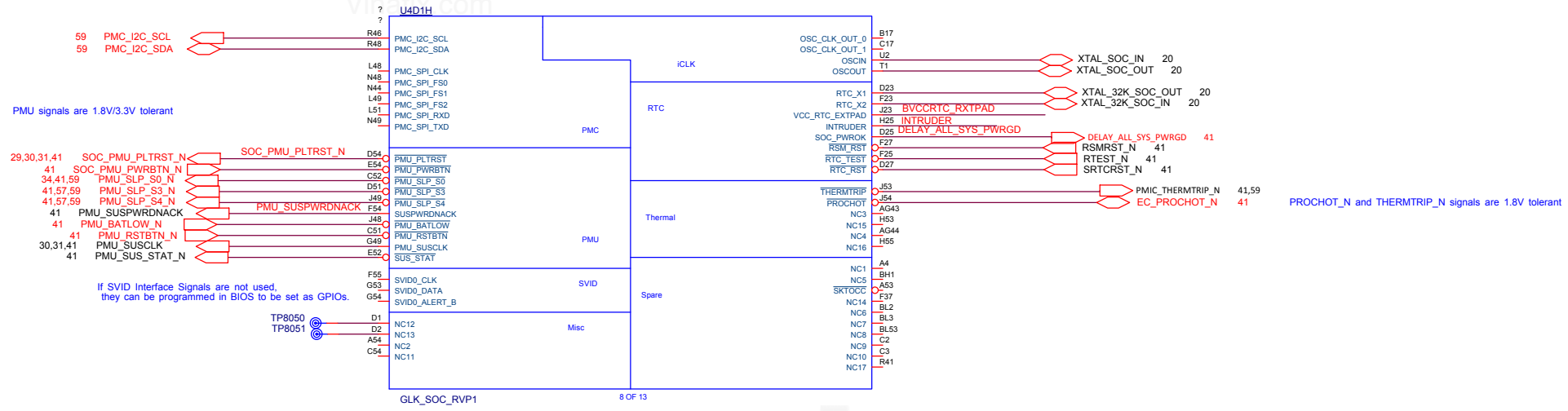
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SOC_SVID&RTC&MISC



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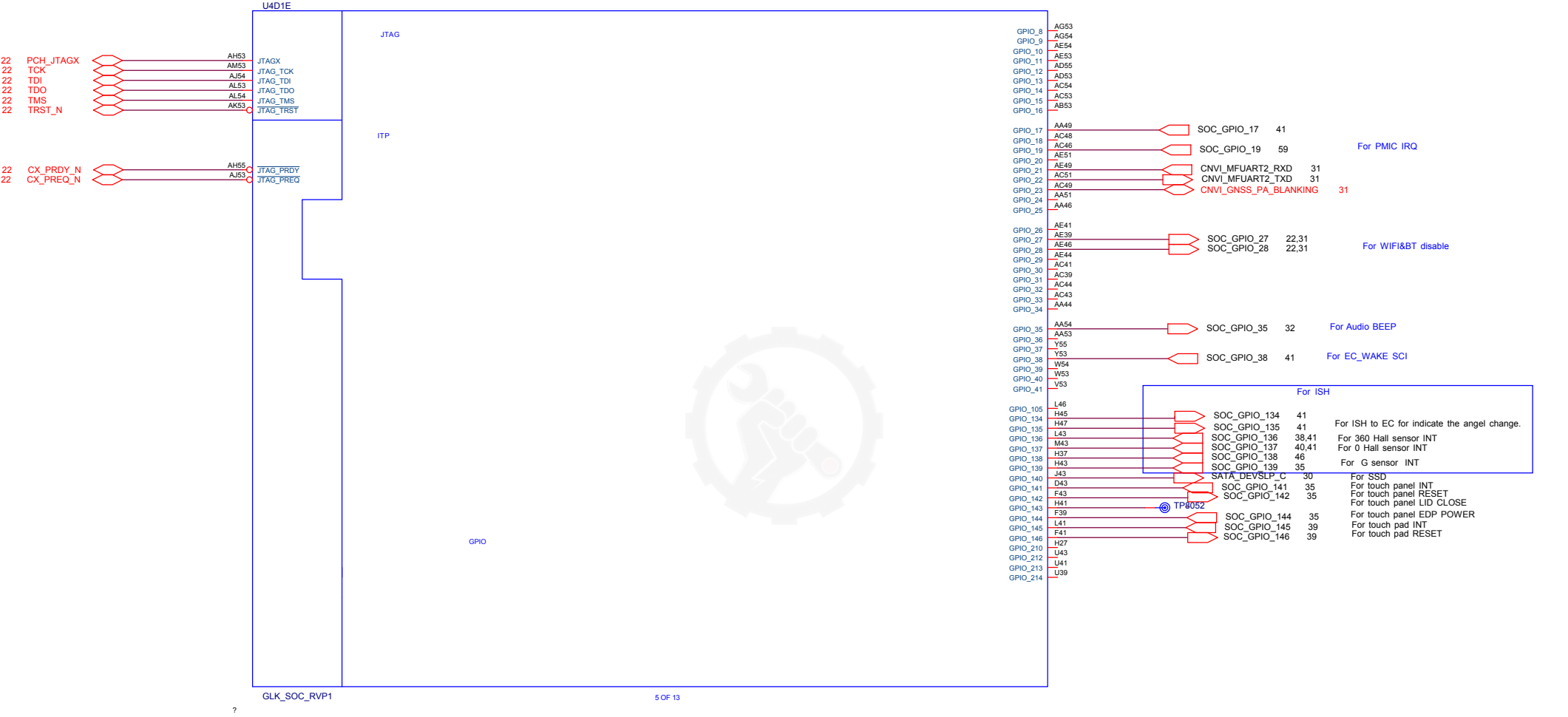
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SOC_GPIO&JTAG&ITP

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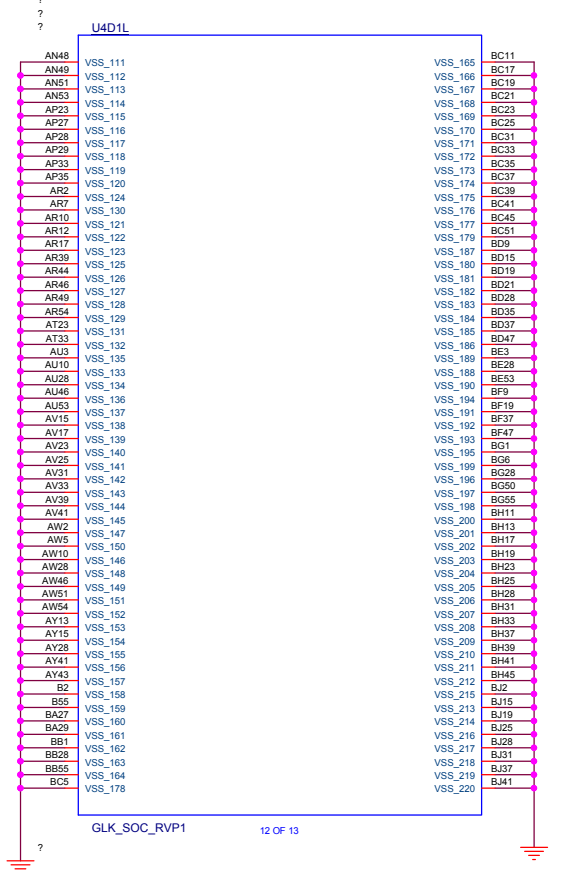
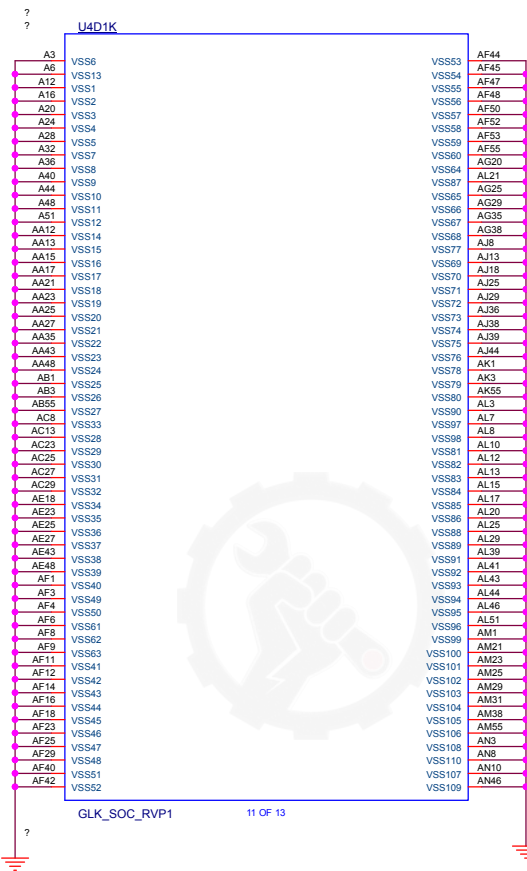
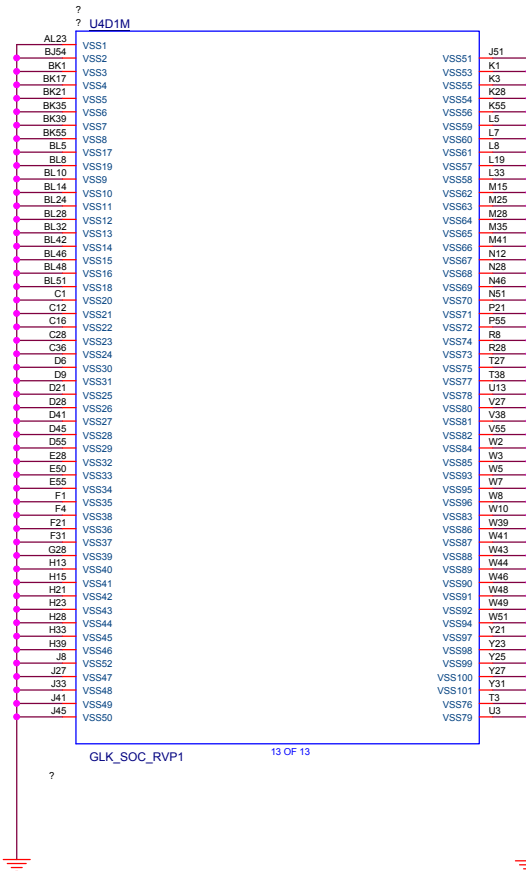
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SOC_GND


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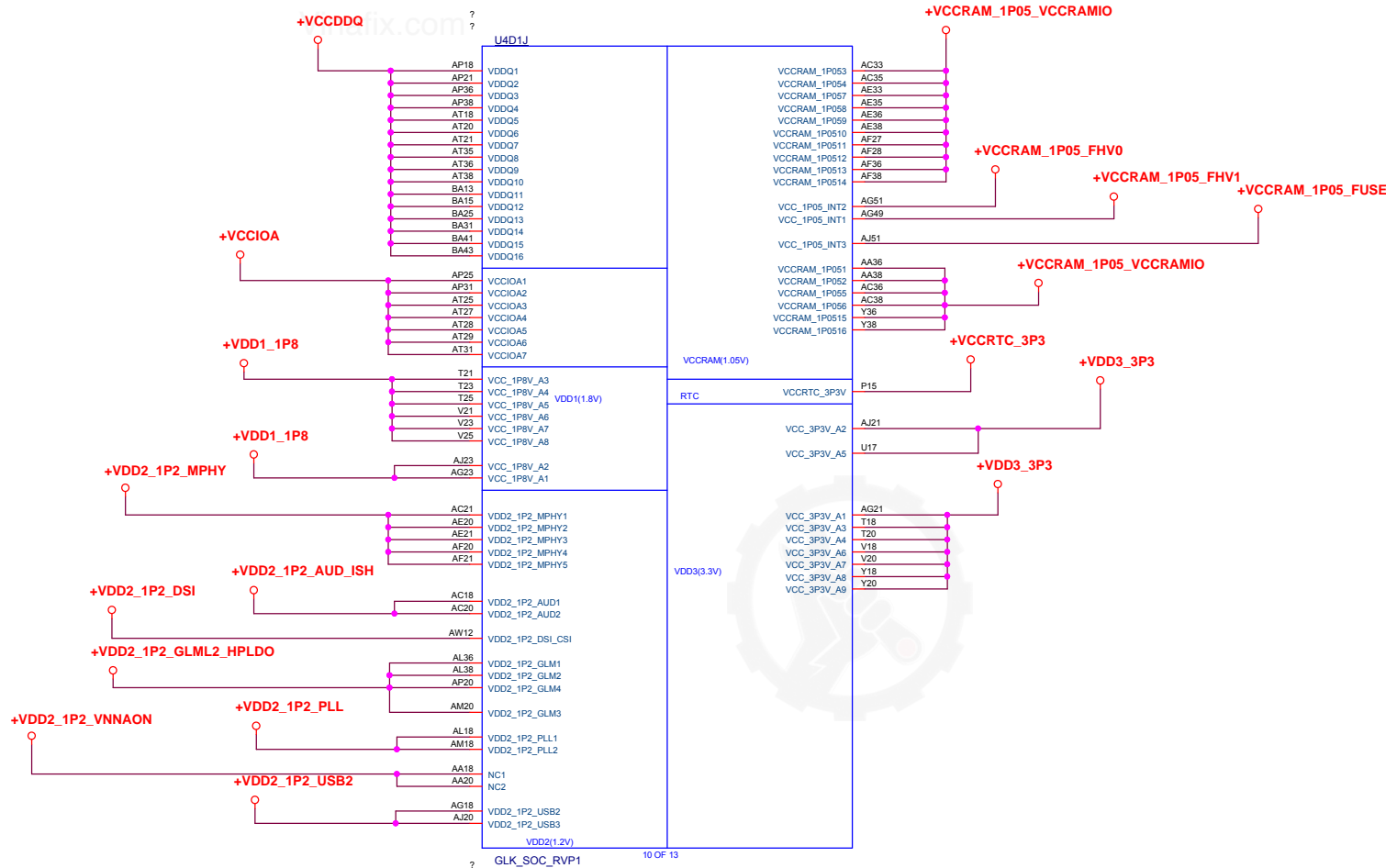
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SOC_POWER SECTION1



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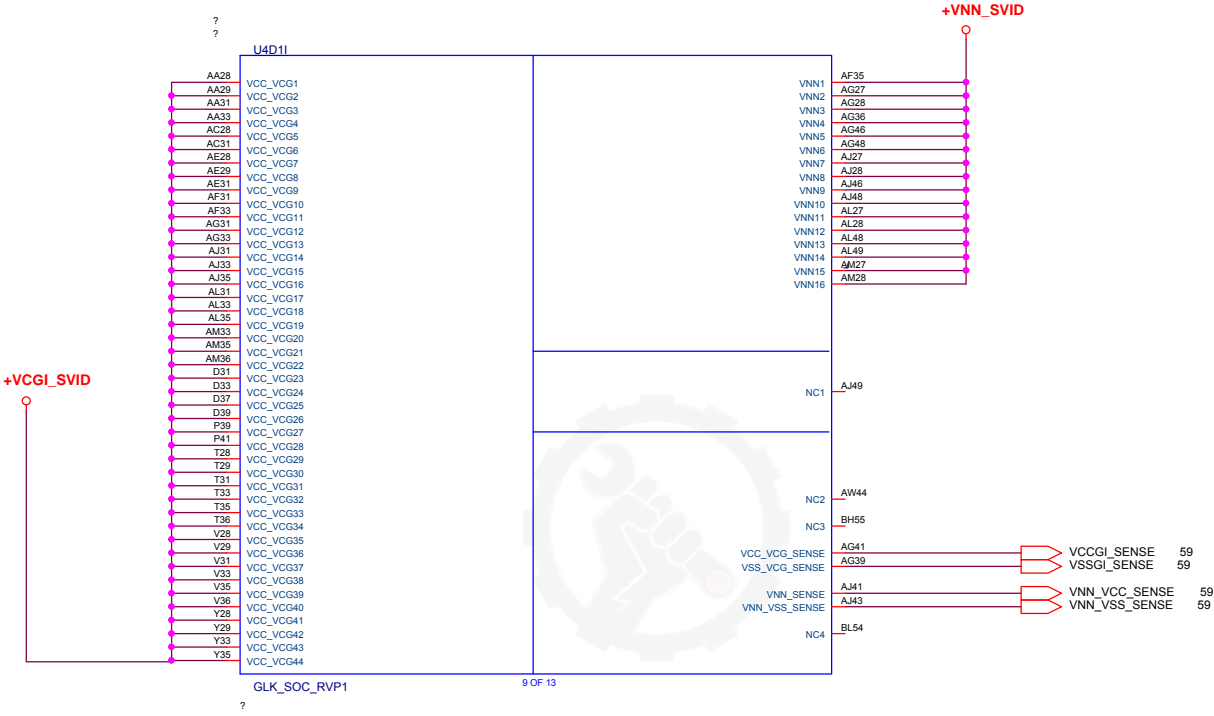
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SOC_POWER SECTION2

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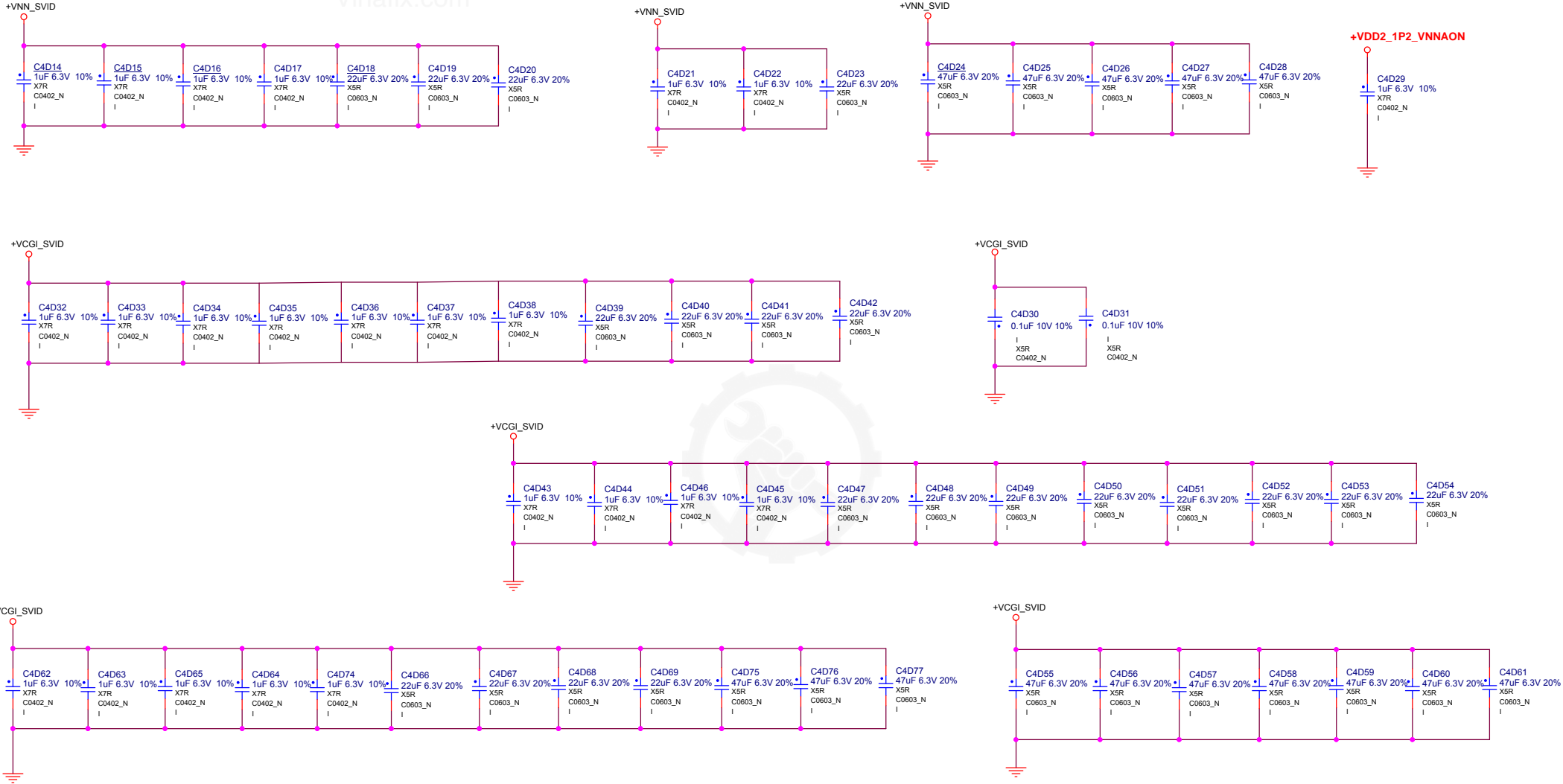
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SOC Power Decoupling

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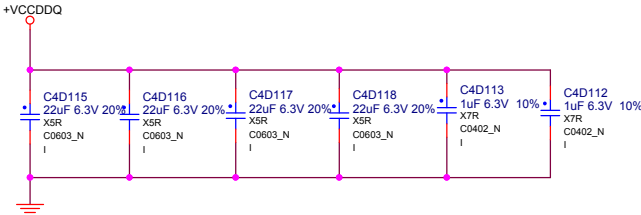
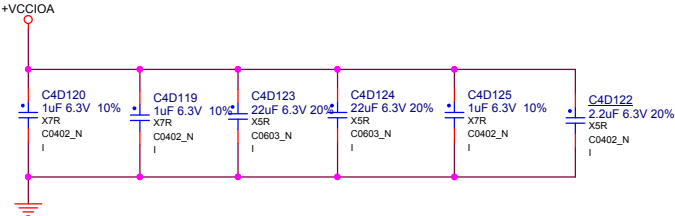
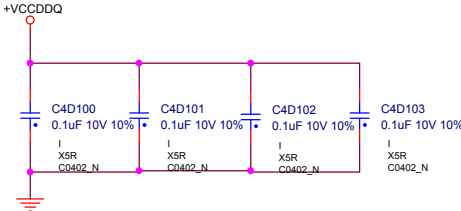
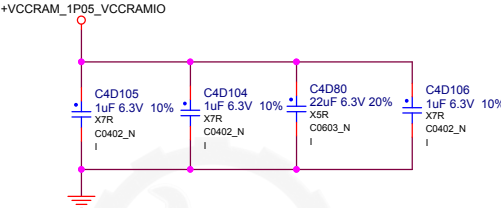
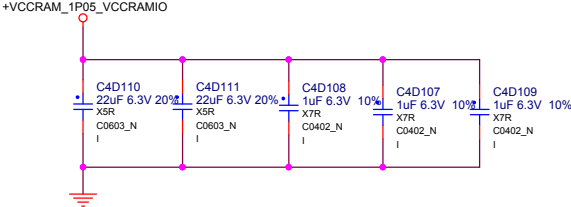
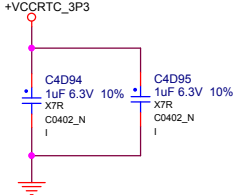
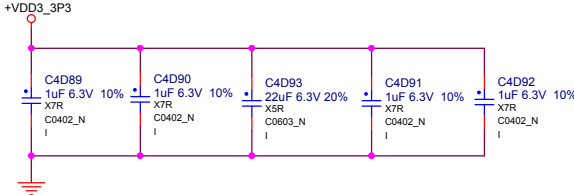
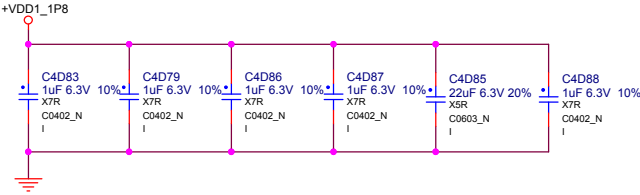
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SOC Power Decoupling

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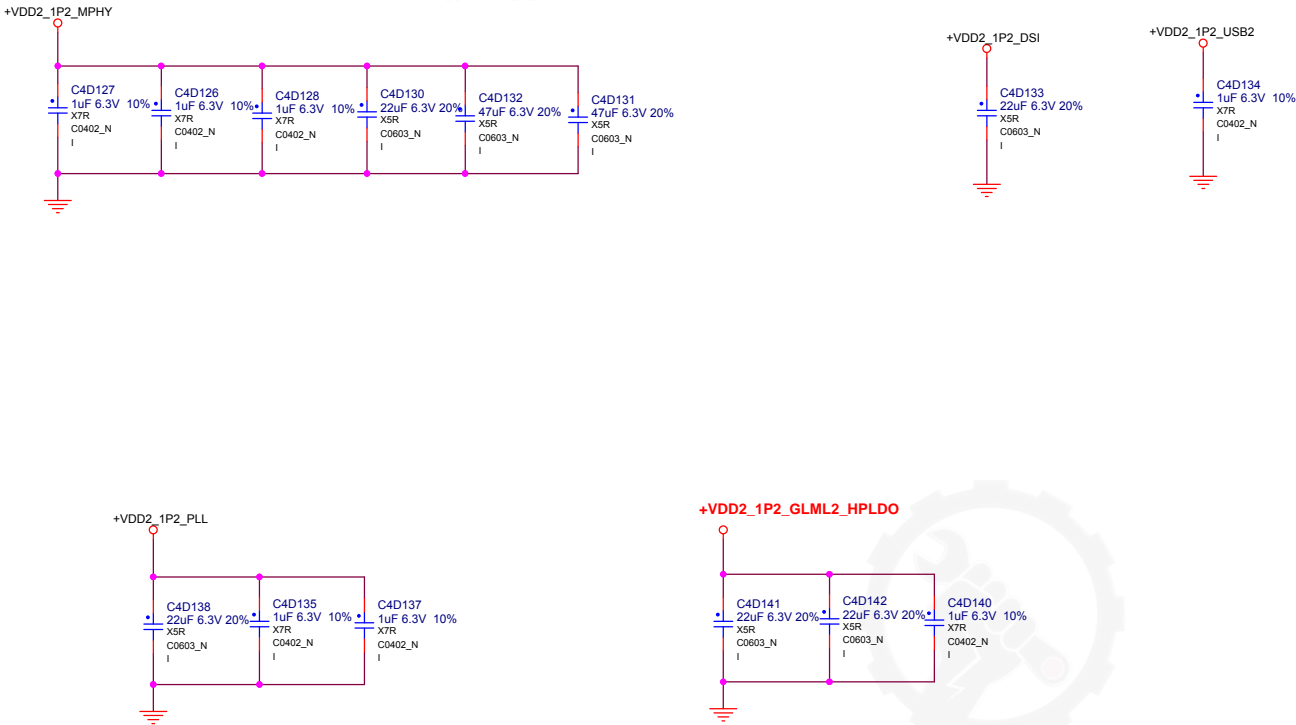
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SOC Power Decoupling

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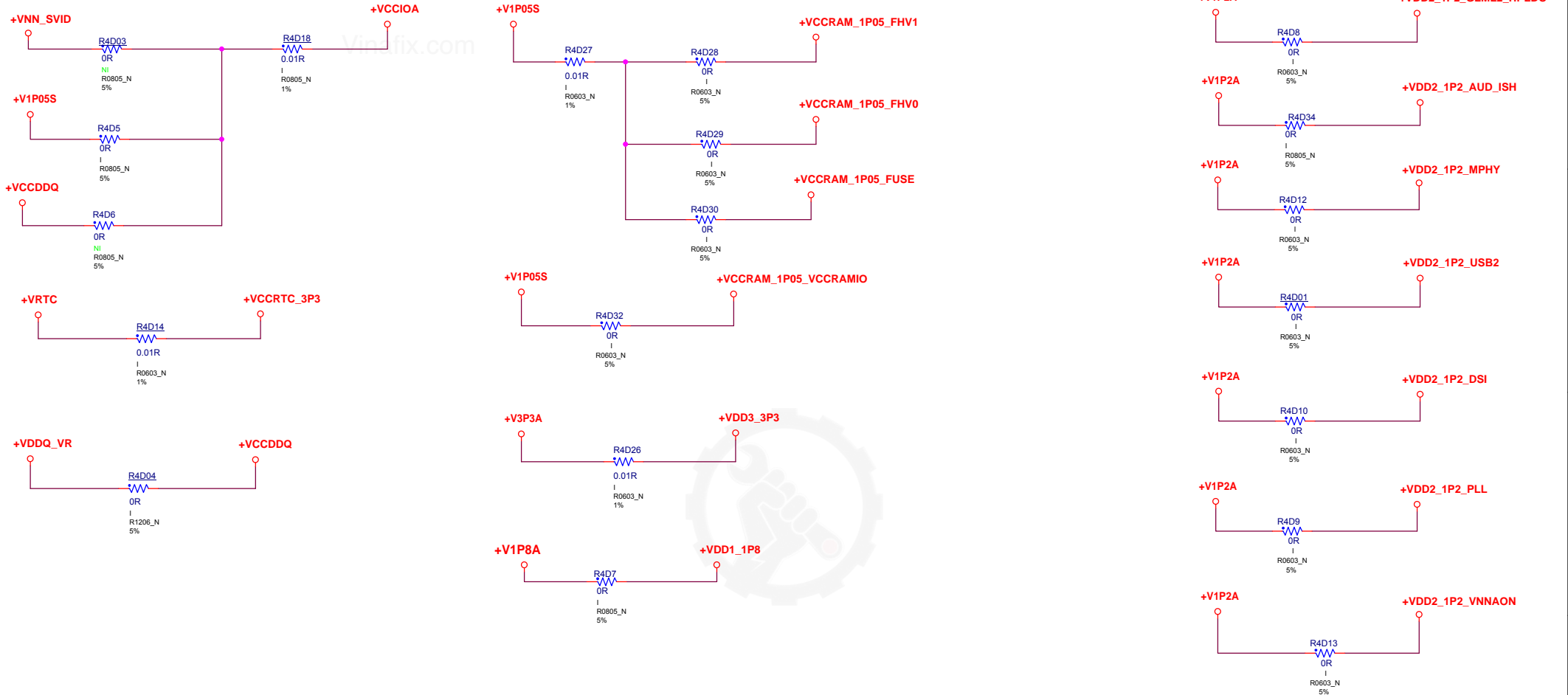
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		V01	


SOC PMR Section



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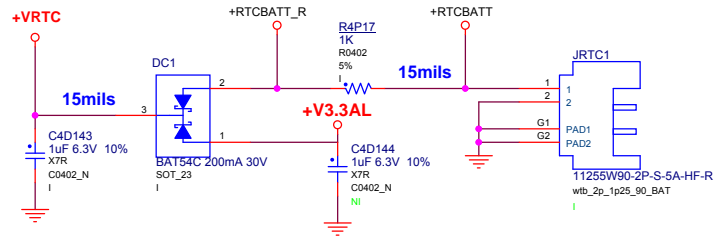
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SOC_XTAL&RTC

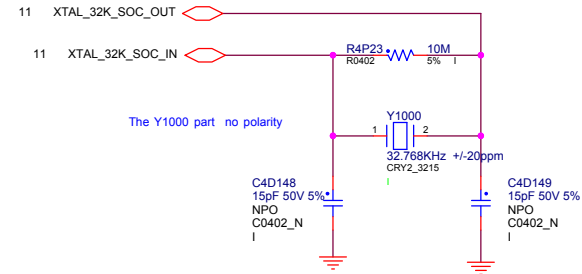
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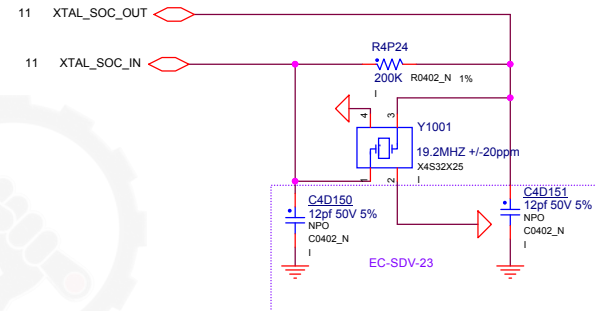
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EC-SIT-05

Change the power rail from +V3P3A to +V3.3AL



The Y1000 part no polarity



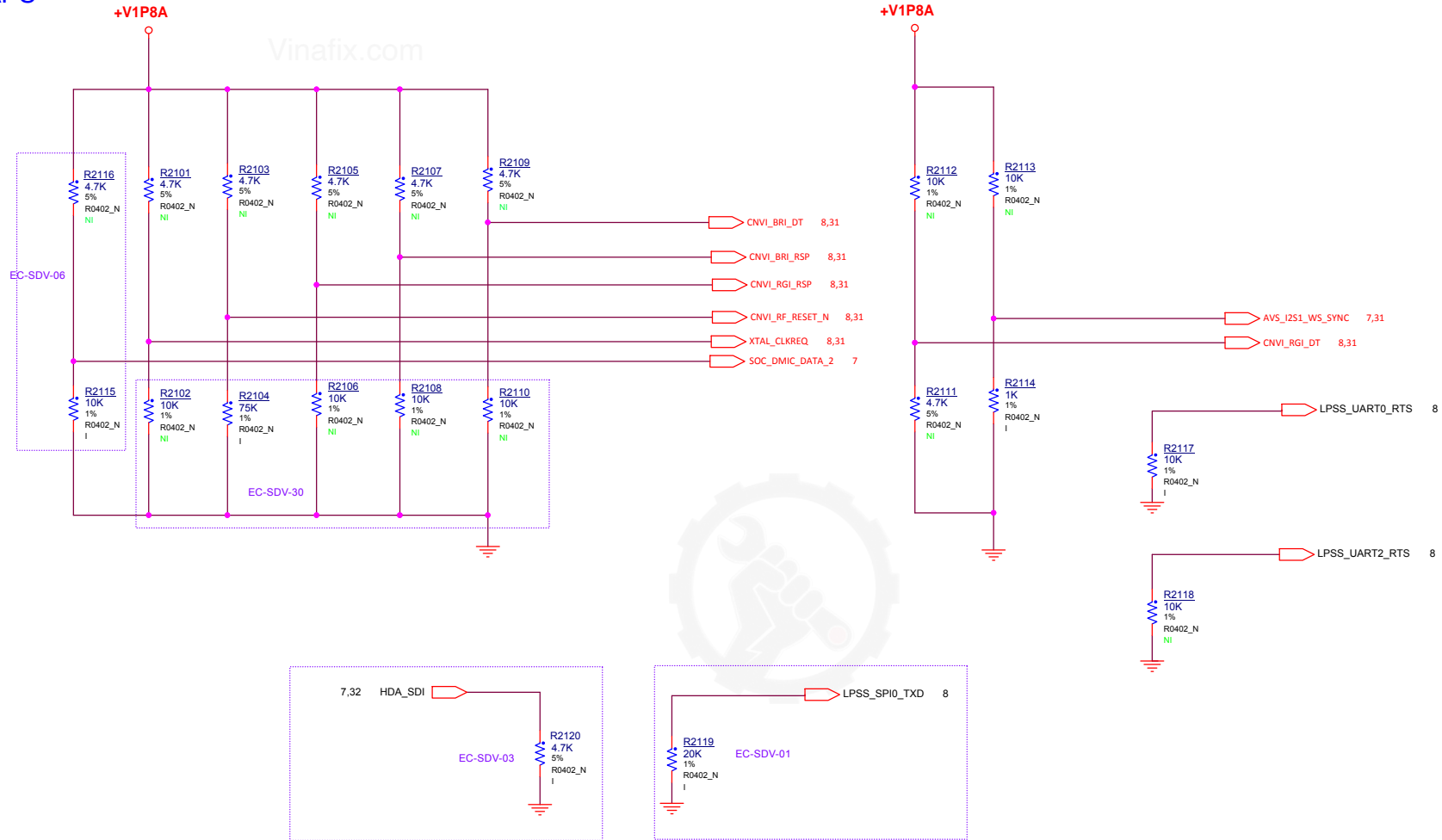
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GLK STRAPS



INTERNAL ONLY

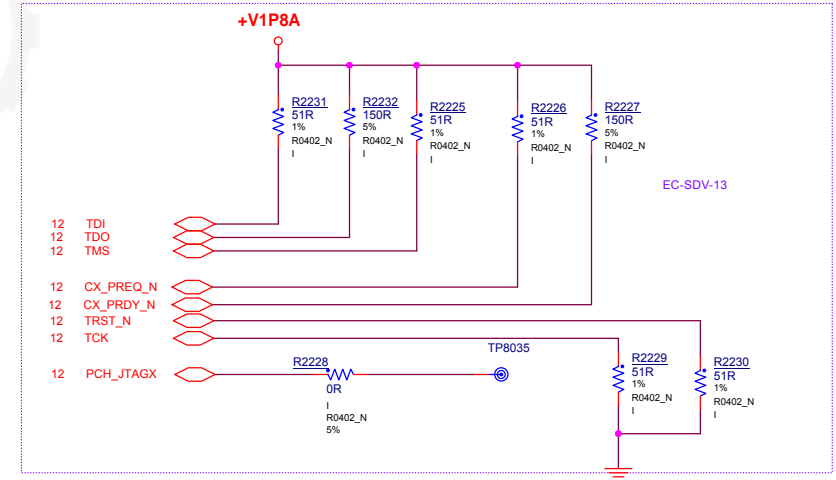
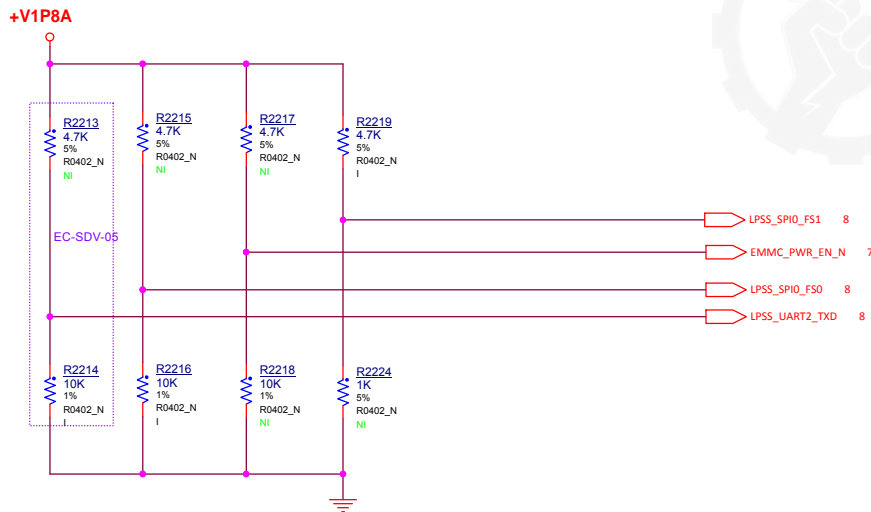
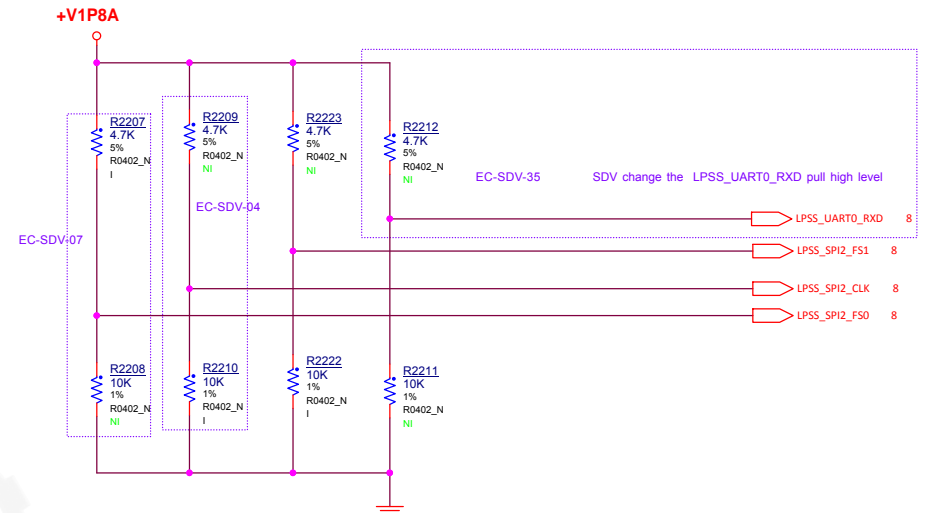
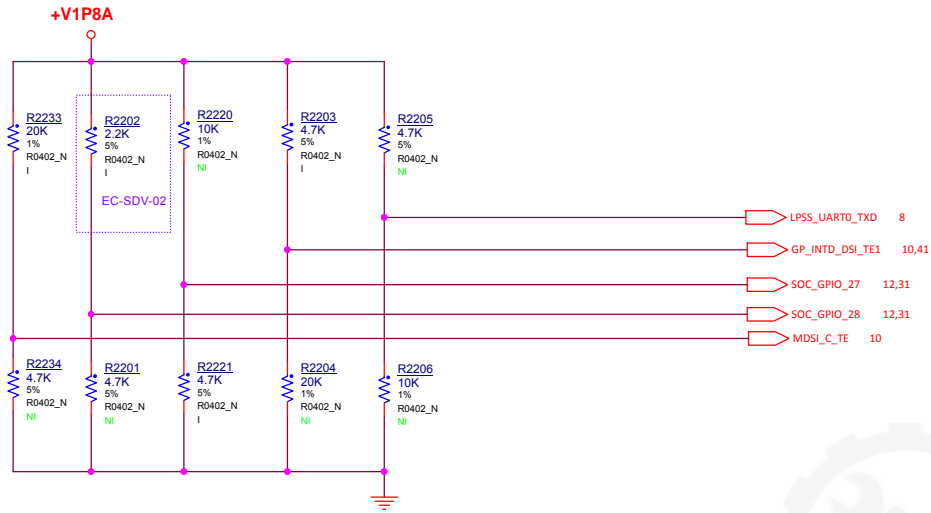
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3nod 三诺		Project: Yoga330	
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GLK_STRAPS

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shy_x_mrd_...
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Project: Yoga330

Engineer: Friendly

Title: GLK_STRAPS

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Size

Custom

Rev

V01

NC


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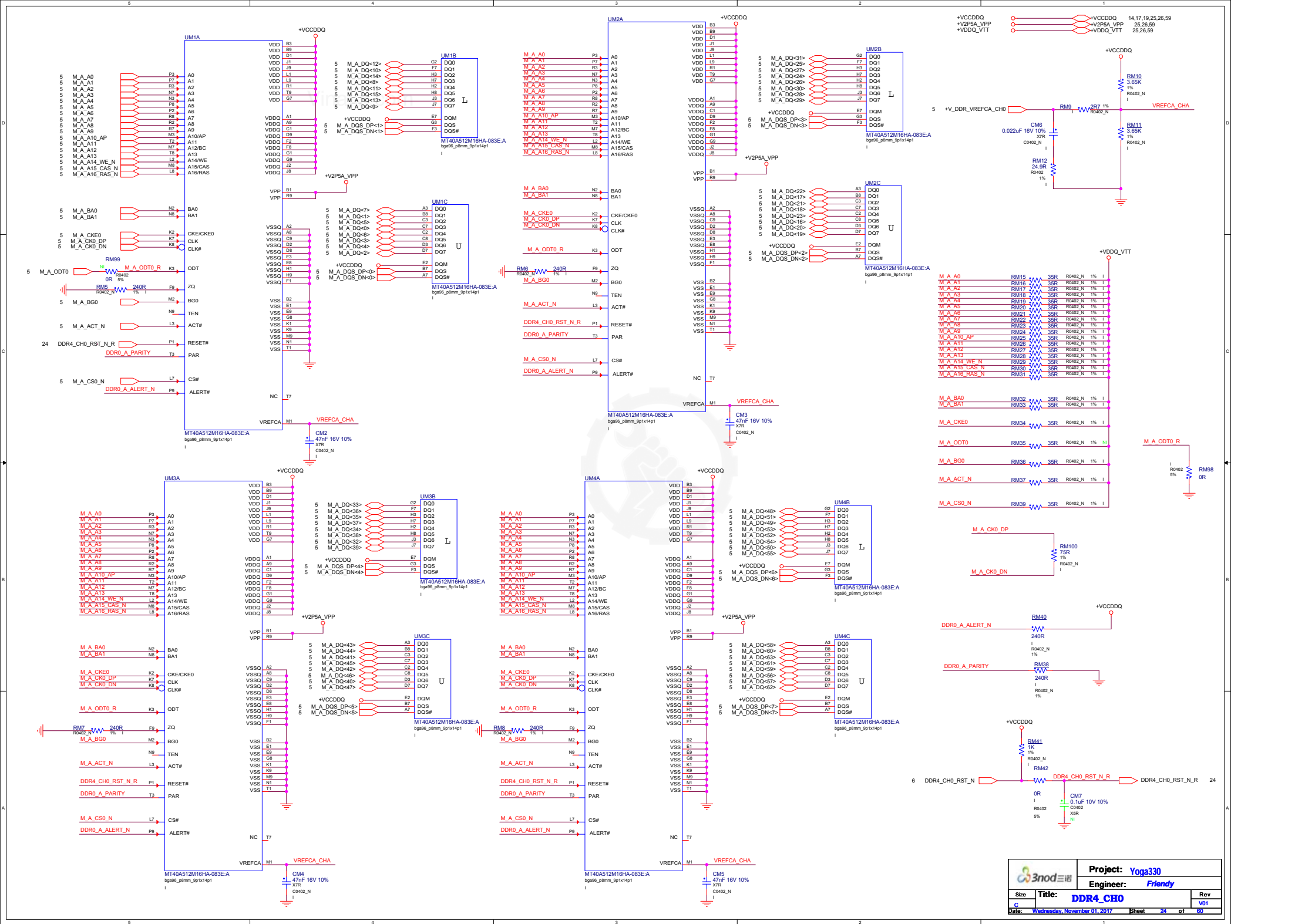


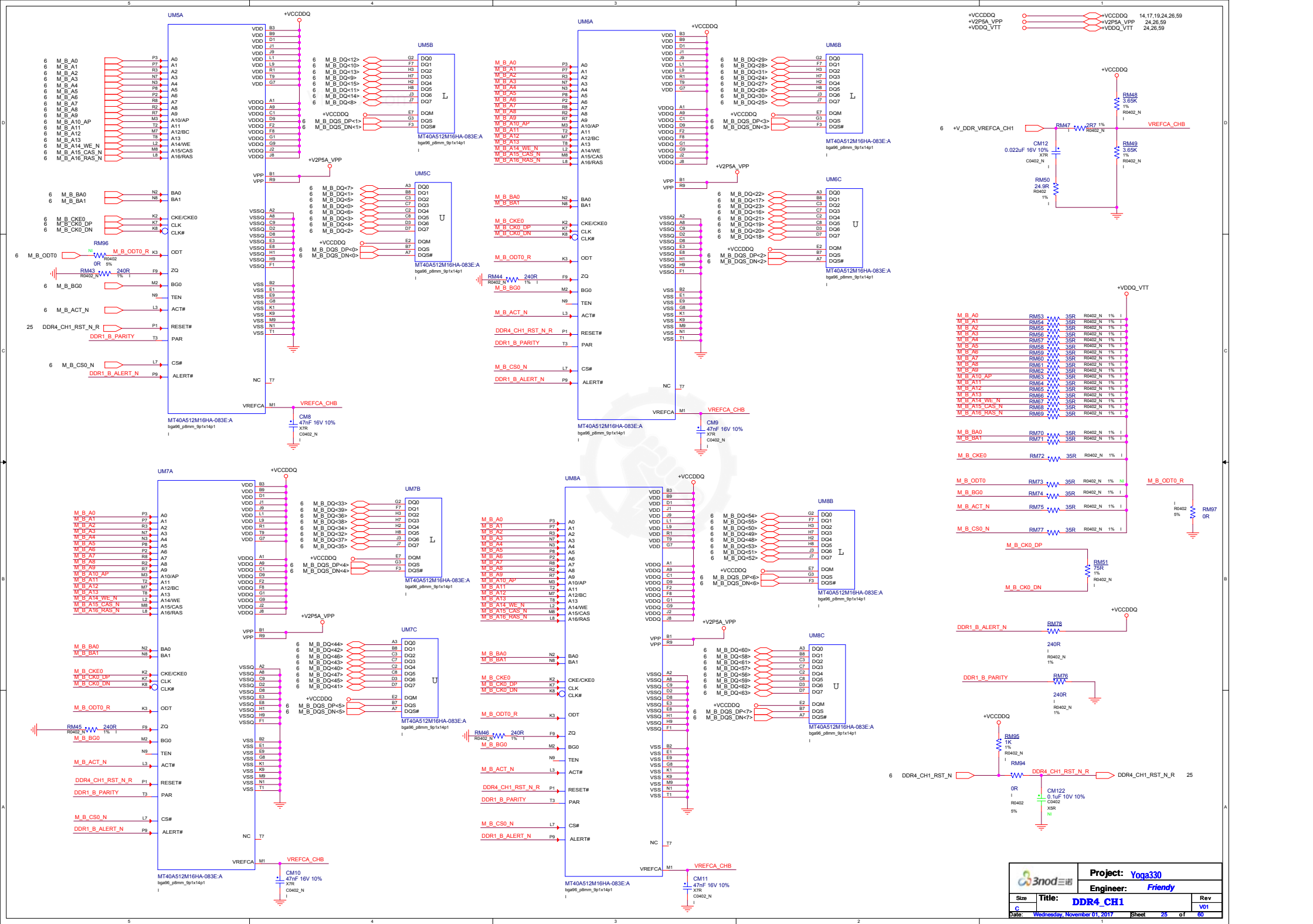
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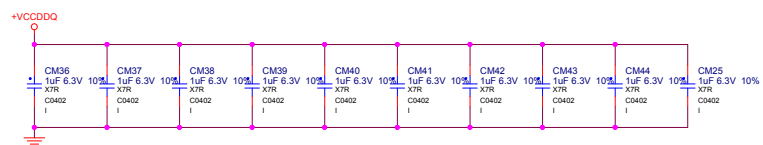
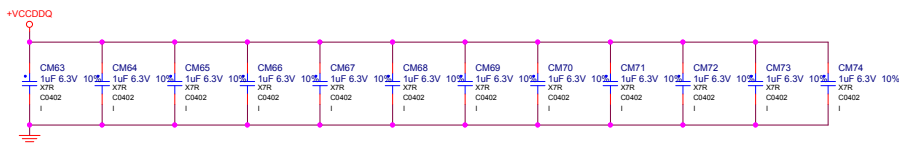
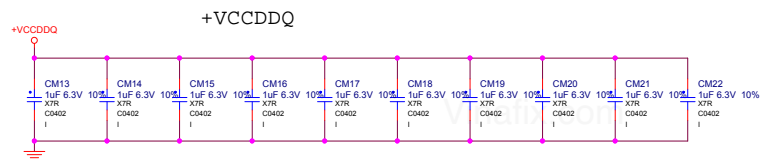
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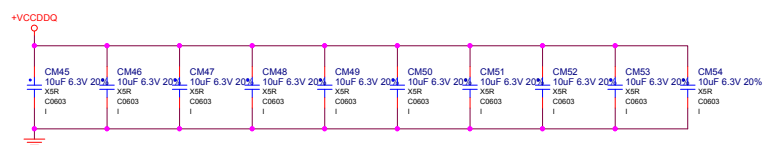
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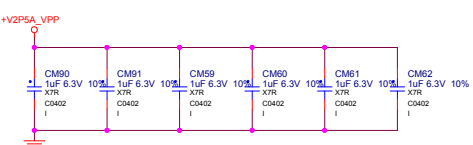
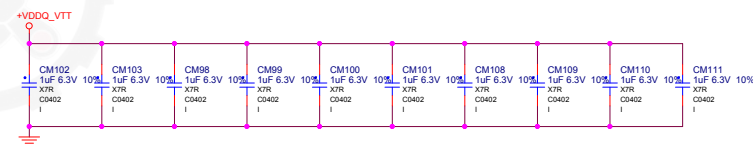
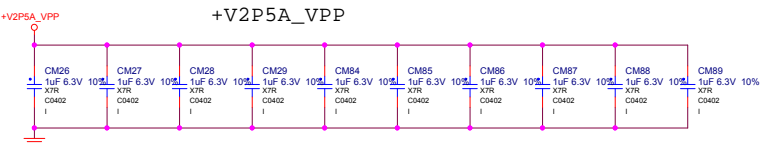
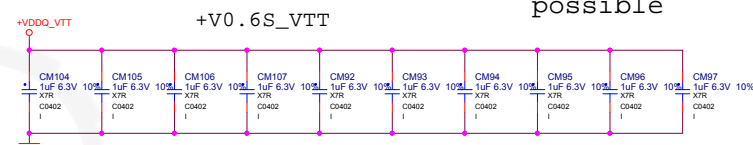


1uF:4 as near each x16
DRAM device as
possible

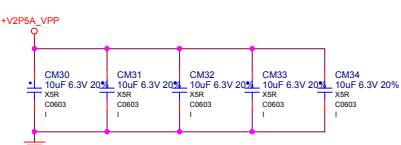
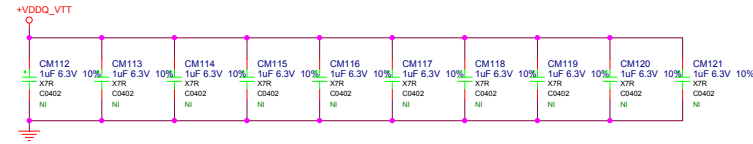


10uF:Distributed around
the DRAM devices

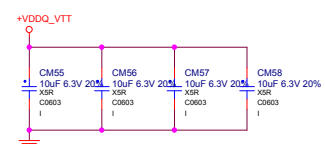
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possible



1uF:2 as near each x16
DRAM device as
possible





10uF:Distributed around
the DRAM devices



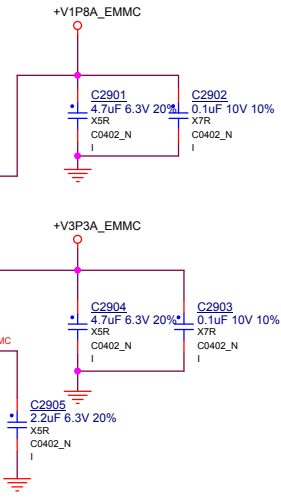
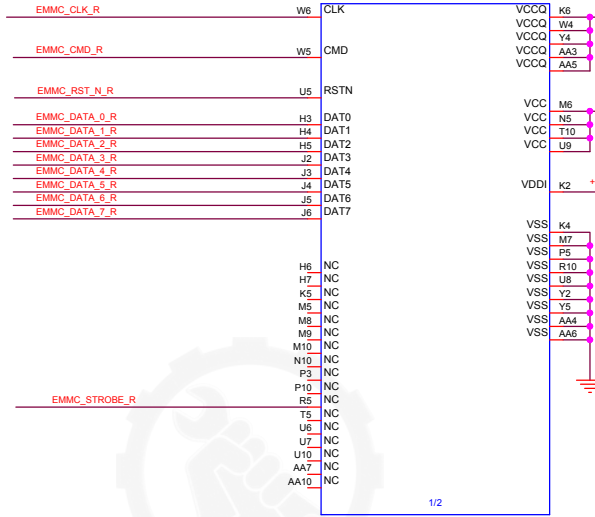
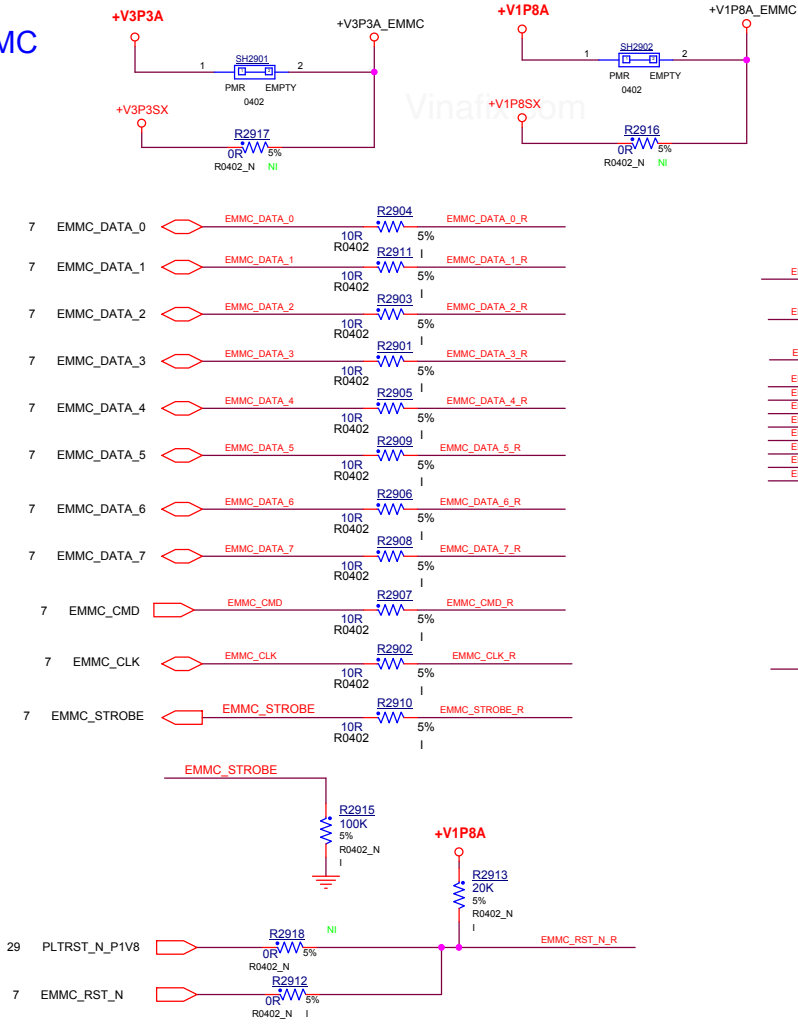
10uF:Distributed around
the DRAM devices

+VCCDDQ 14,17,19,24,25,59
+V2P5A_VPP 24,25,59
+VDDQ_VTT 24,25,59

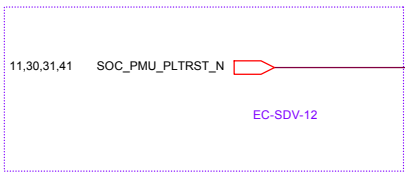
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D	Vinafix.com								D
C									C
B									B
A									A
INTERNAL ONLY				BPAGE DRAWING					
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8	7	6	5	4	3	2	1		

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		Engineer: Friendly	
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EMMC



U2901B		
NCEMBS99		
A4	NC_1	NC_40
A11	NC_41	L3
B2	NC_5	NC_41
B13	NC_6	NC_42
D1	NC_7	L12
D14	NC_8	NC_43
H1	NC_9	L13
H2	NC_10	NC_44
Y7	NC_100	M1
Y8	NC_101	NC_45
Y9	NC_102	M2
Y10	NC_103	NC_46
Y11	NC_104	M3
Y12	NC_105	NC_47
Y13	NC_106	M12
Y14	NC_107	NC_48
AA1	NC_108	M13
AA2	NC_109	NC_49
H8	NC_11	M14
AA8	NC_110	NC_50
AA9	NC_111	N1
AA11	NC_112	NC_51
AA12	NC_113	N2
AA13	NC_114	NC_52
AA14	NC_115	N3
AE1	NC_116	N12
AE14	NC_117	NC_53
AG2	NC_118	N13
AG13	NC_119	N14
H9	NC_12	P1
AH4	NC_120	P2
AH6	NC_121	P12
AH9	NC_122	P13
AH11	NC_123	P14
H10	NC_13	R1
H11	NC_14	NC_62
H12	NC_15	R2
H13	NC_16	NC_63
H14	NC_17	R3
J1	NC_18	NC_64
J7	NC_19	R12
A6	NC_2	NC_65
J8	NC_20	R13
J9	NC_21	R14
J10	NC_22	T1
J11	NC_23	NC_69
J12	NC_24	T2
J13	NC_25	NC_70
J14	NC_26	T3
K1	NC_27	T12
K3	NC_28	T13
A9	NC_3	T14
K7	NC_30	U1
K8	NC_31	NC_74
K9	NC_32	U2
K10	NC_33	NC_75
K11	NC_34	U3
K12	NC_35	U12
K13	NC_36	U13
K14	NC_37	U14
L1	NC_38	V1
L2	NC_39	NC_81
		Y3
		NC_82
		V12
		NC_83
		V13
		NC_84
		V14
		NC_85
		W1
		NC_86
		W2
		NC_87
		W3
		NC_88
		W7
		NC_89
		W8
		NC_90
		W9
		NC_91
		W10
		NC_92
		W11
		NC_93
		W12
		NC_94
		W13
		NC_95
		W14
		NC_96
		Y1
		NC_97
		Y3
		NC_98
		Y6
		NC_99

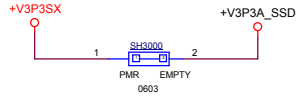


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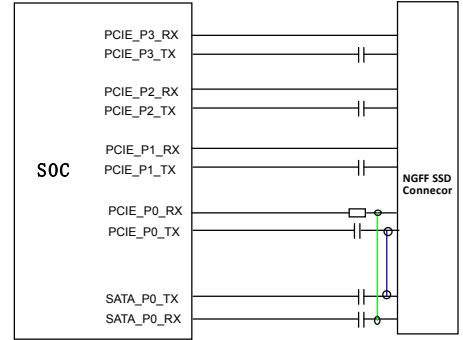
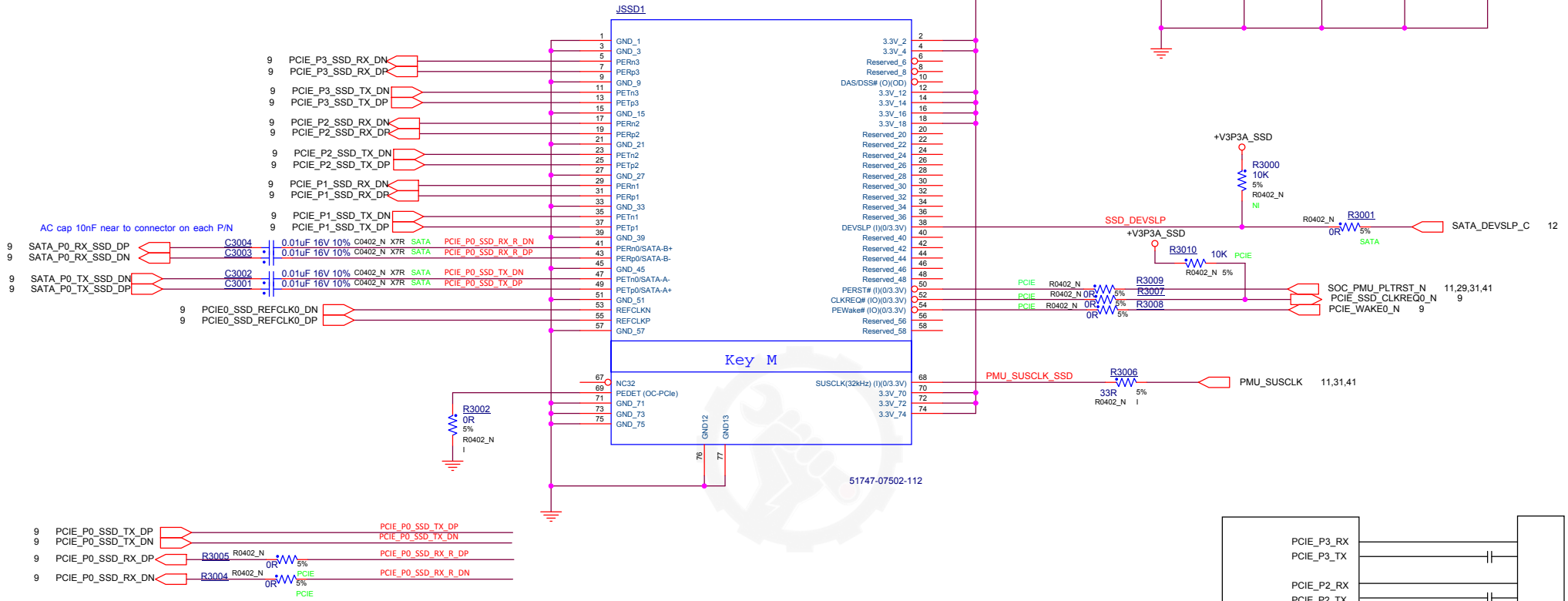
3nod 三诺		Project: Yoga330	
Size: Custom		Engineer: Friendly	
Title: EMMC		Rev: V01	
Date: Wednesday, November 01, 2017		Sheet 29 of 60	

SSD



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SSD M.2 CONN



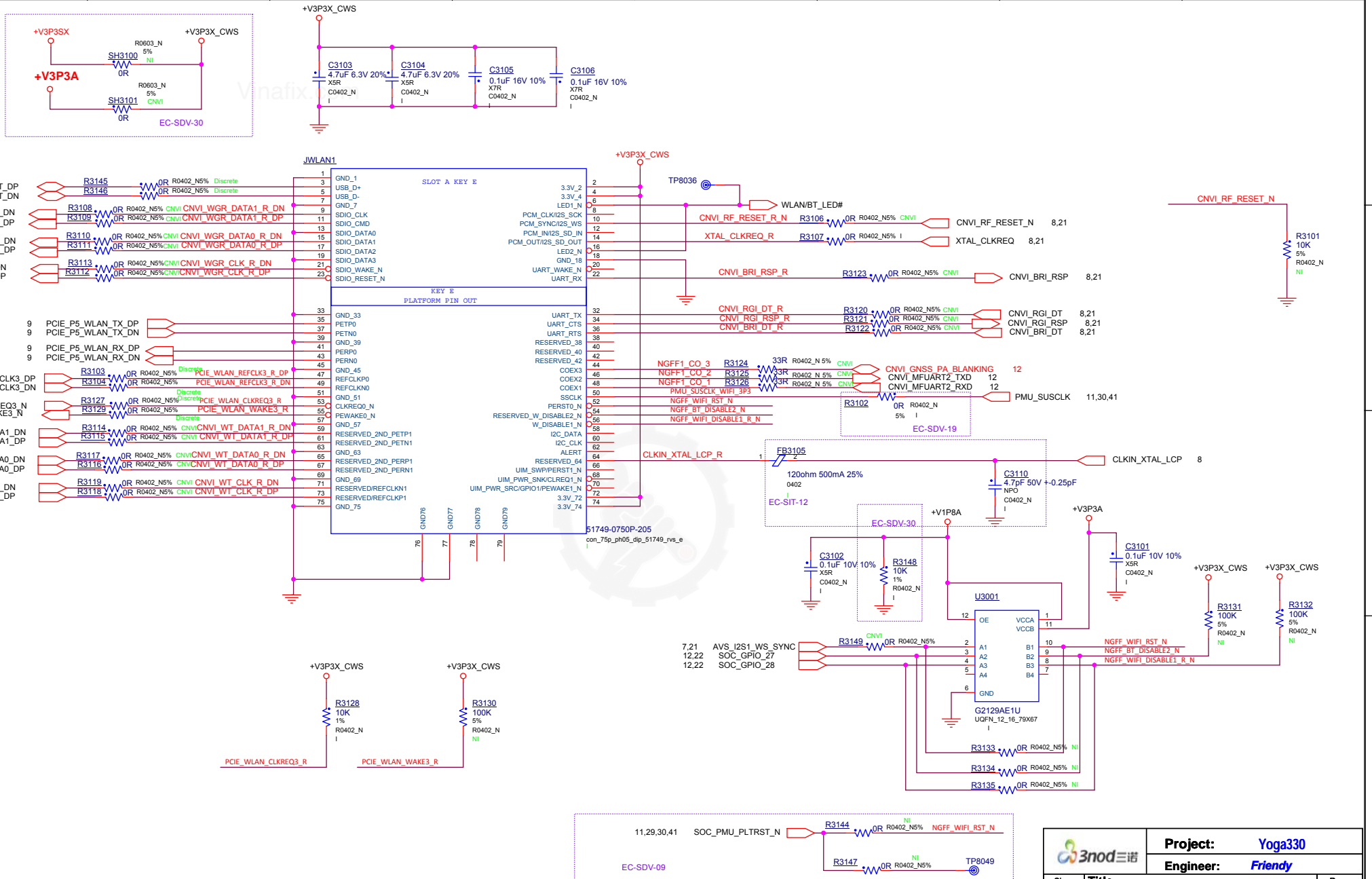
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Wed Jun 03 11:22:42 2015

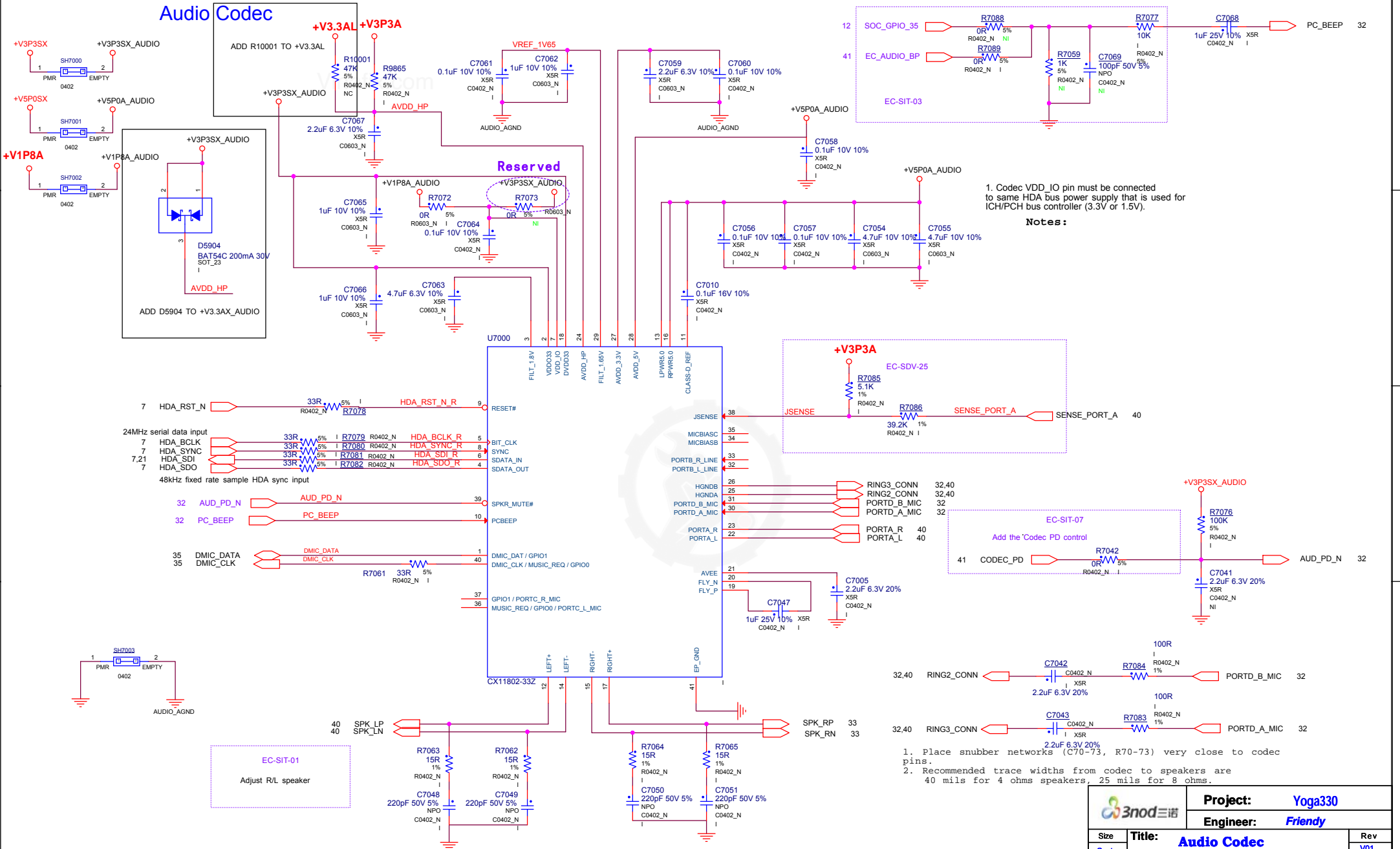
		Project: Yoga330	
Size: Custom		Engineer: Friendly	
Title: SSD		Rev: V01	
Date: Wednesday, November 01, 2017		Sheet 30 of 60	

WIFI&BT



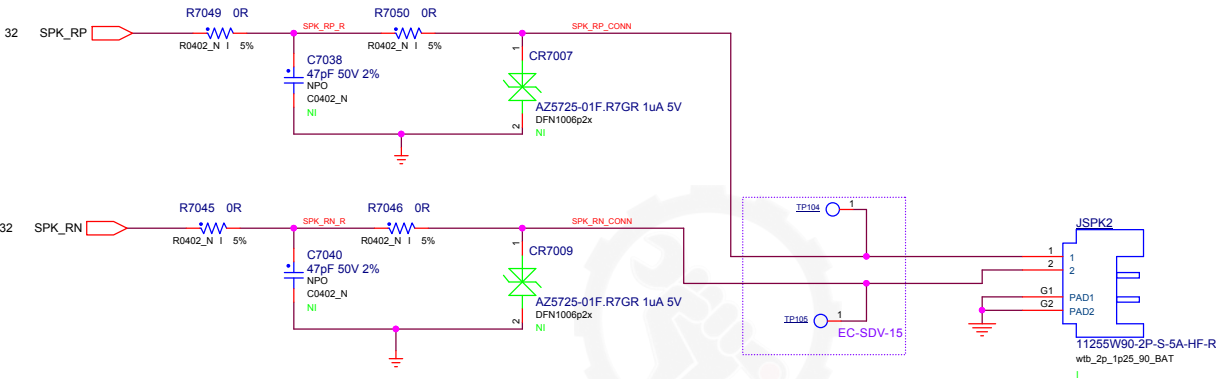
 3nod 三诺		Project: <i>Yoga330</i>	
		Engineer: <i>Friendly</i>	
Size	Title: <i>WiFi&BT</i>	Rev	
Custom		V01	
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Audio Codec



HEADSET JACK (Supports CTIA and OMTP headsets)

Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.

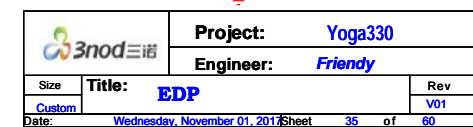


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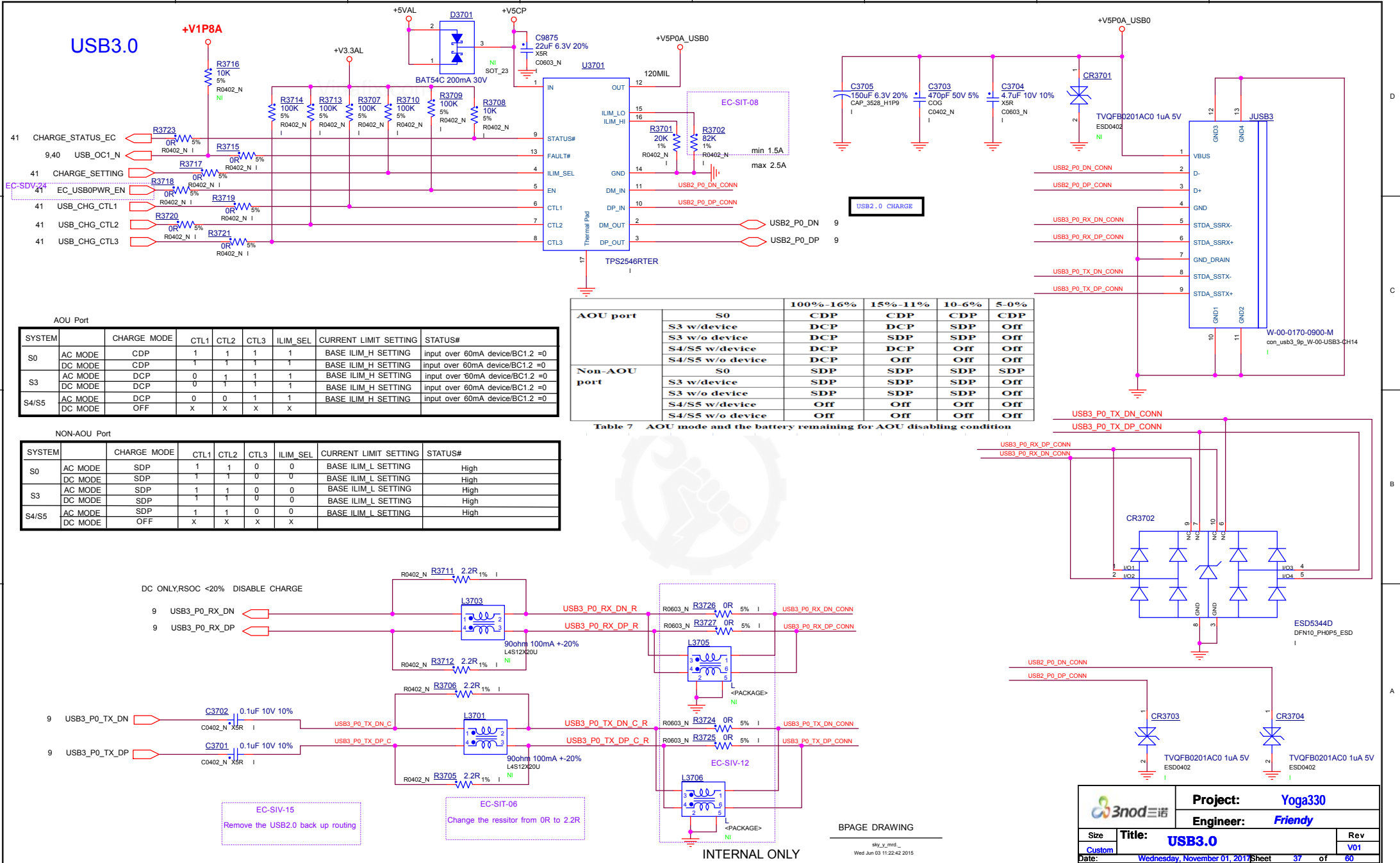
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		Project: Yoga330	
Size		Engineer: Friendly	
Custom	Title: Audio SPK	Rev	V01
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USB3.0



AOU Port							
SYSTEM		CHARGE MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	AC MODE	CDP	1	1	1	1	BASE ILIM_H SETTING
	DC MODE	CDP	1	1	1	1	BASE ILIM_H SETTING
S3	AC MODE	DCP	0	1	1	1	BASE ILIM_H SETTING
	DC MODE	DCP	0	1	1	1	BASE ILIM_H SETTING
S4/S5	AC MODE	DCP	0	0	1	1	BASE ILIM_H SETTING
	DC MODE	OFF	X	X	X	X	BASE ILIM_H SETTING

Non-AOU Port							
SYSTEM		CHARGE MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	AC MODE	SDP	1	1	0	0	BASE ILIM_L SETTING
	DC MODE	SDP	1	1	0	0	BASE ILIM_L SETTING
S3	AC MODE	SDP	1	1	0	0	BASE ILIM_L SETTING
	DC MODE	SDP	1	1	0	0	BASE ILIM_L SETTING
S4/S5	AC MODE	SDP	1	1	0	0	BASE ILIM_L SETTING
	DC MODE	OFF	X	X	X	X	BASE ILIM_L SETTING

AOU port	S0	100%-16%	15%-11%	10-6%	5-0%
	S3 w/device	CDP	CDP	CDP	CDP
Non-AOU port	S3 w/o device	DCP	DCP	SDP	Off
	S4/S5 w/device	DCP	DCP	SDP	Off
	S4/S5 w/o device	DCP	Off	Off	Off
	S4/S5 w/o device	Off	Off	Off	Off

Table 7 AOU mode and the battery remaining for AOU disabling condition

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Project: Yoga330	
Engineer: Friendly	
Size: Custom	Title: USB3.0
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Thermal Sensor

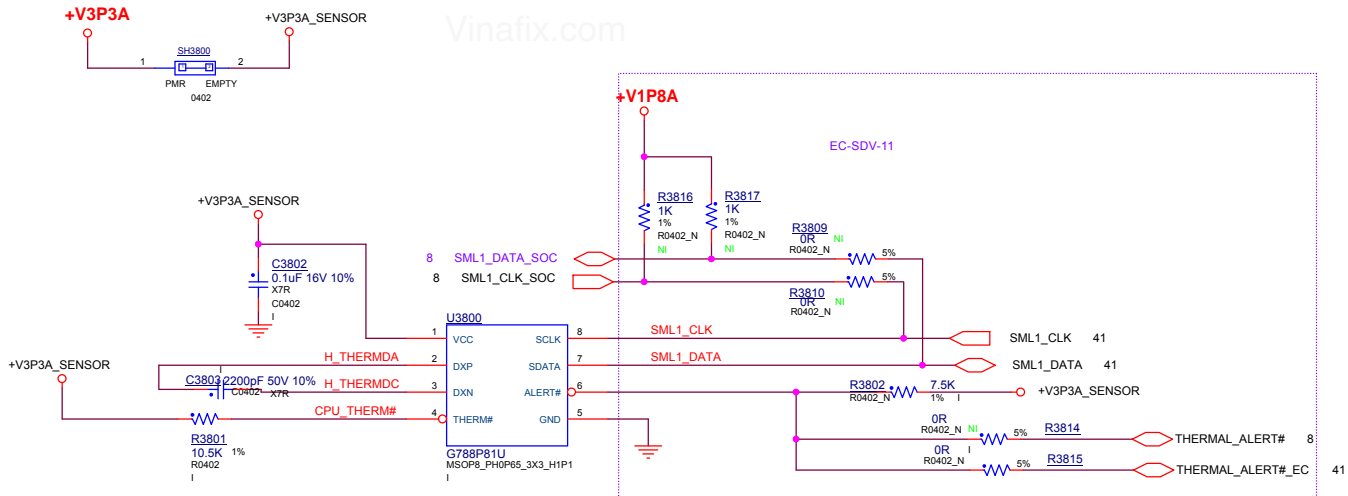
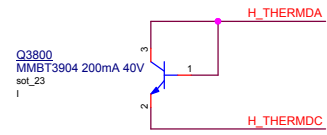
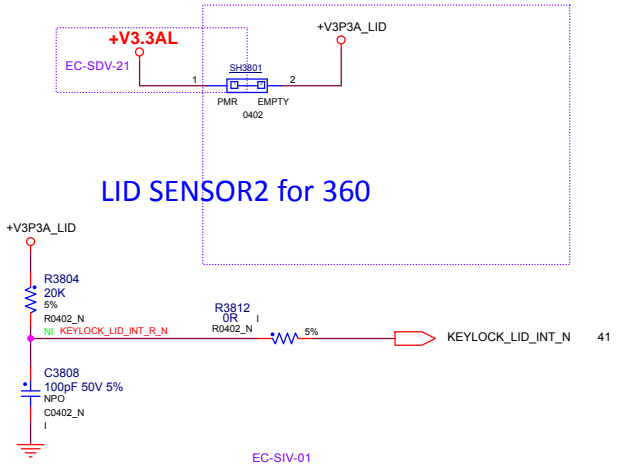


Table 10. Remote temperature THERM limit
The default value is trapping after power up 100ms by different pull-up resistors of THERM and ALERT pin:

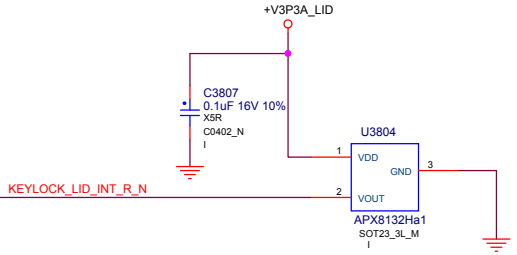
TEMPERATURE (°C)	THERM					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



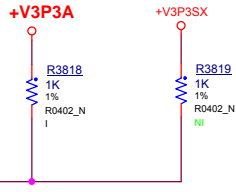
LID SENSOR1 for 0----remove to IO board



LID SENSOR2 for 360



EC-SIT-10
change the hall sensor INT to EC, then EC to SOC



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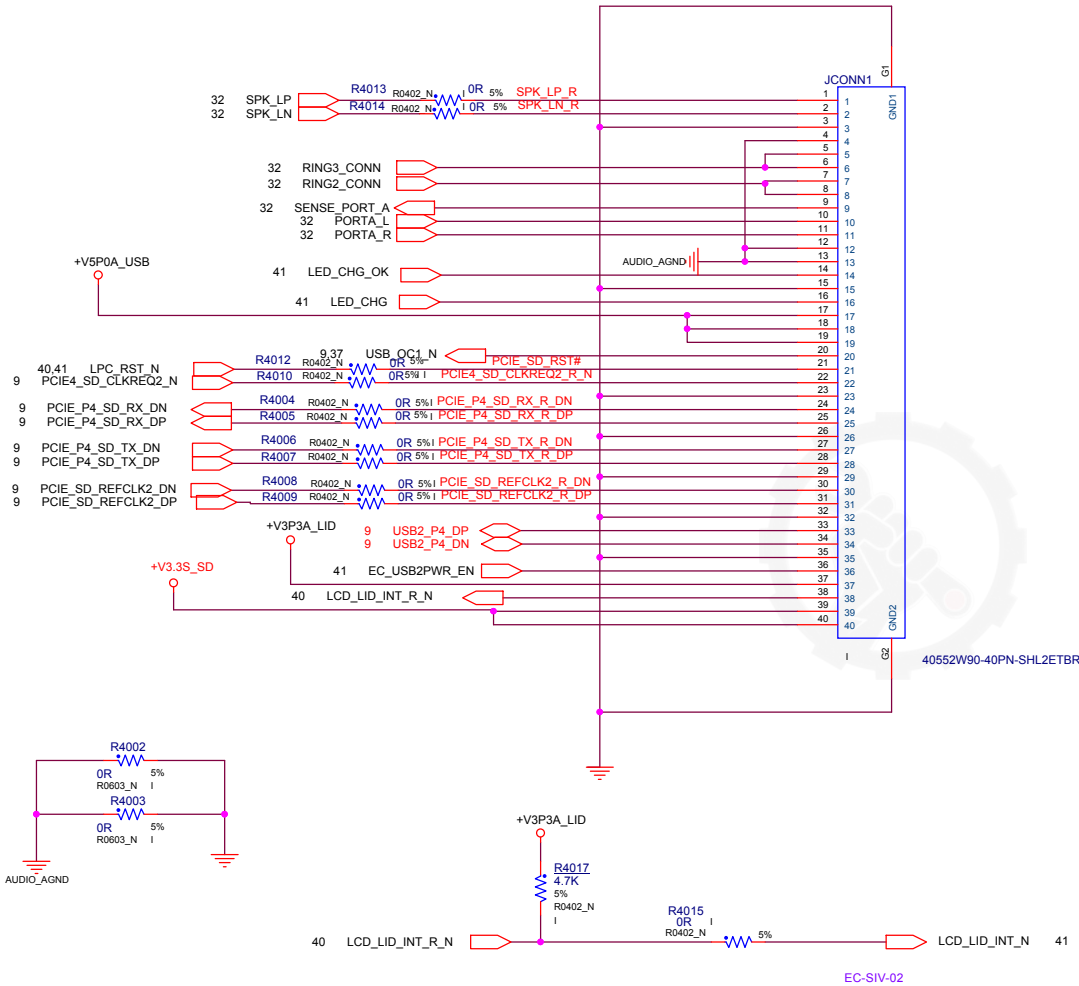
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Wed Jun 03 11:22:42 2015

Project: Yoga330
Engineer: Friendly

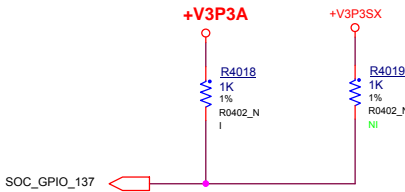
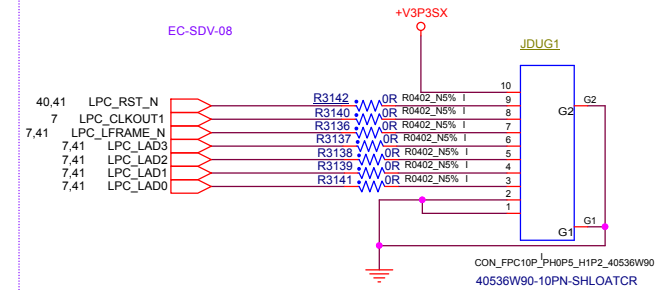
Size: Custom
Title: Sensors
Date: Wednesday, November 01, 2017

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IO Connector



Debug Connector



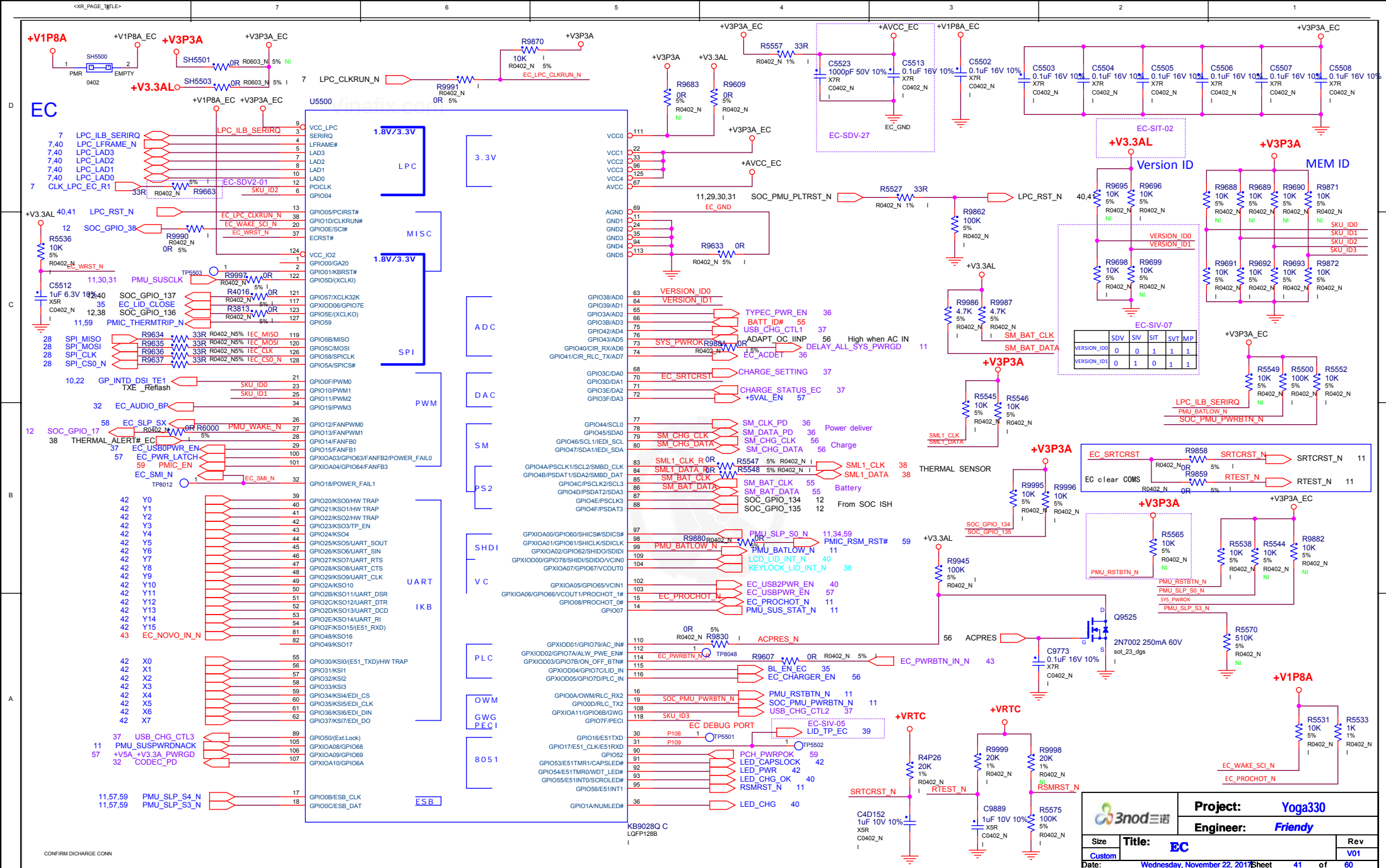
EC-SIT-10
change the hall sensor INT to EC, then EC to SOC

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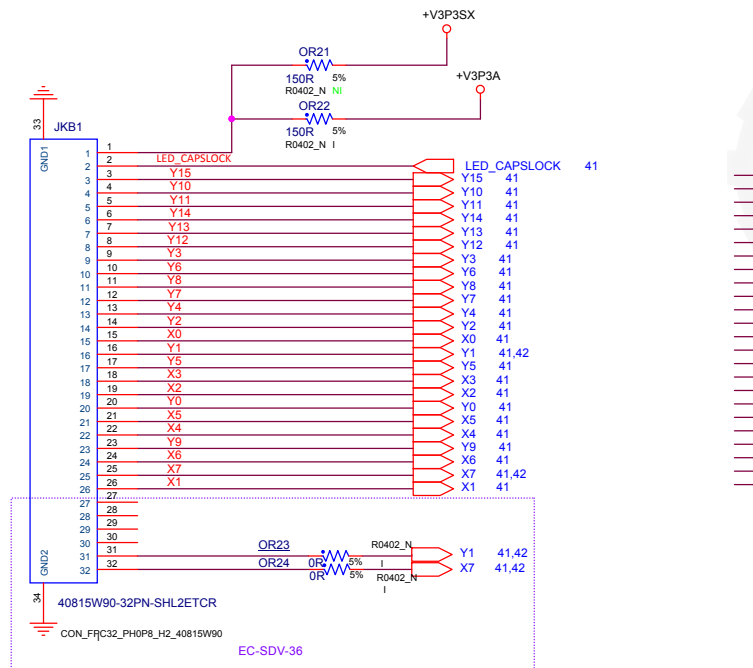
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Wed Jun 03 11:22:42 2015

3nod 三诺		Project: Yoga330	
Size: Custom		Engineer: Friendly	
Title: IO		Rev: V01	
Date: Wednesday, November 01, 2017		Sheet 40 of 60	




PWR LED



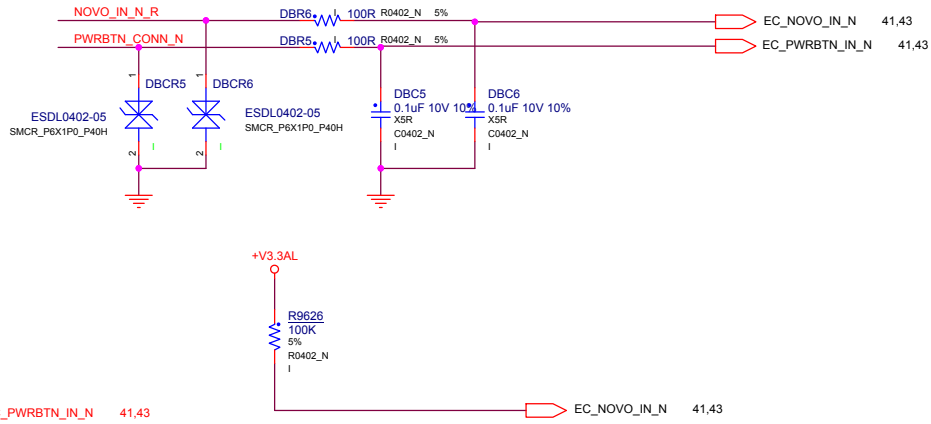
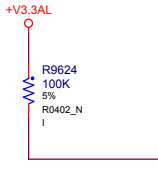
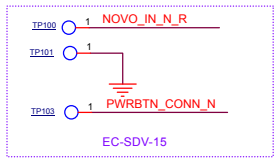
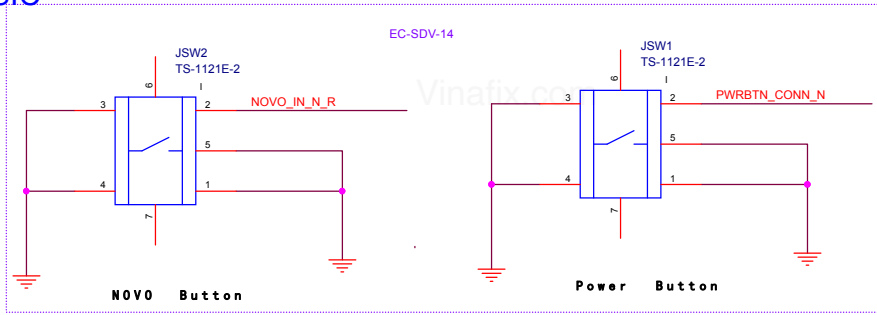
Y15	C10	1000pF	50V	10%	C0402	X	NR	NI
Y10	C11	1000pF	50V	10%	C0402	X	NR	NI
Y11	C12	1000pF	50V	10%	C0402	X	NR	NI
Y14	C13	1000pF	50V	10%	C0402	X	NR	NI
Y15	C14	1000pF	50V	10%	C0402	X	NR	NI
Y12	C15	1000pF	50V	10%	C0402	X	NR	NI
Y3	C16	1000pF	50V	10%	C0402	X	NR	NI
Y6	C17	1000pF	50V	10%	C0402	X	NR	NI
Y8	C18	1000pF	50V	10%	C0402	X	NR	NI
Y19	C19	1000pF	50V	10%	C0402	X	NR	NI
Y4	C20	1000pF	50V	10%	C0402	X	NR	NI
Y2	C21	1000pF	50V	10%	C0402	X	NR	NI
X0	C22	1000pF	50V	10%	C0402	X	NR	NI
Y1	C23	1000pF	50V	10%	C0402	X	NR	NI
X4	C24	1000pF	50V	10%	C0402	X	NR	NI
X3	C25	1000pF	50V	10%	C0402	X	NR	NI
X2	C26	1000pF	50V	10%	C0402	X	NR	NI
X0	C27	1000pF	50V	10%	C0402	X	NR	NI
Y5	C28	1000pF	50V	10%	C0402	X	NR	NI
X8	C29	1000pF	50V	10%	C0402	X	NR	NI
X9	C30	1000pF	50V	10%	C0402	X	NR	NI
X6	C31	1000pF	50V	10%	C0402	X	NR	NI
X7	C32	1000pF	50V	10%	C0402	X	NR	NI
X1	C33	1000pF	50V	10%	C0402	X	NR	NI

NOVO Button

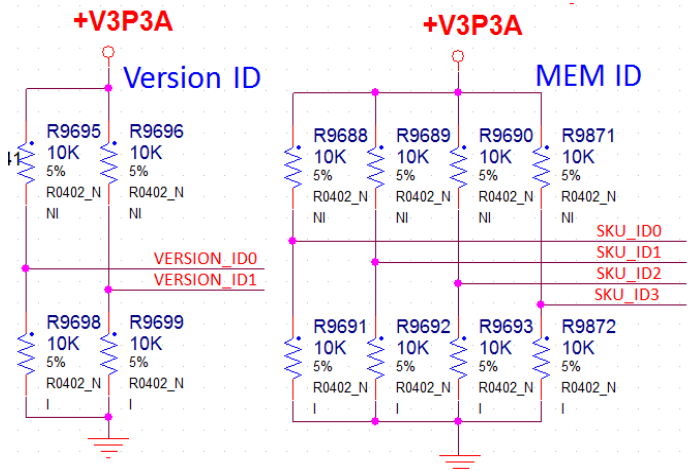
sky_y_mrd._ apl_ff.UN\$14.141
Wed Jun 03 11:22:42 2015

		Project: <i>Yoga330</i>	
		Engineer: <i>Friendly</i>	
Size	Title: <i>EC</i>	Rev	
<i>Custom</i>		<i>V01</i>	
Date: <i>Wednesday, November 01, 2017</i>		Sheet <i>42</i>	of <i>60</i>

MSIC



ID configuration



version ID

version ID	SDV	SIV	SIT	SVT	MP
VERSION_ID0	0	0	1	1	0
VERSION_ID1	0	1	1	0	0
R9695	NI	NI	I	I	NI
R9696	NI	I	I	NI	NI
R9698	I	I	NI	NI	I
R9699	I	NI	NI	I	I

Memory ID

Memory ID	Samsung 4GB	Hynix 4GB	Micron 4GB	Samsung 8GB	Hynix 8GB	Micron 8GB	single channel Samsung 4GB	single channel Hynix 4GB	single channel Micron 4GB	Samsung 2GB	Hynix 2GB	Micron 2GB
SKU_ID0	0	0	0	0	0	0	0	0	1	1	1	1
SKU_ID1	0	0	0	0	1	1	1	1	0	0	0	1
SKU_ID2	0	0	1	1	0	0	1	1	0	0	1	0
SKU_ID3	0	1	0	1	0	1	0	1	0	1	1	0
R9688	NI	NI	NI	NI	NI	NI	NI	NI	NI	NI	NI	NI
R9691	I	I	I	I	I	I	I	I	I	I	I	I
R9689	NI	NI	NI	NI	I	I	NI	NI	NI	NI	NI	NI
R9692	I	I	I	I	NI	NI	I	I	I	I	I	I
R9690	NI	NI	I	I	NI	NI	NI	NI	NI	NI	NI	NI
R9693	I	I	NI	NI	I	I	I	I	I	I	I	I
R9871	NI	I	NI	I	NI	NI	NI	NI	NI	NI	NI	NI
R9872	I	NI	I	NI	I	I	I	I	I	I	I	I

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		Engineer: Friendly	
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Notes:

1. All the straps are sampled at Rising Edge of KSM_RST_N
2. The internal termination value listed in this table will be in effect before and until

Table 2-28. Hardware Straps (Sheet 1 of 3)

LPID #	File Name	Pathname	Internal Extension	File Name Storage/Encryption/Policy
GP21_17	GP21_17	Global Admin. as a super user	209 PLS	1 - Create 2 - Create a new file for this device. 3 - Create a pull-down for the disk to display EPHC 4 - Create a pull-down for the disk to display EPHC
GP21_18	GP21_18	Global Admin. as a super user	209 PLS	1 - Create 2 - Create a new file for this device. 3 - Create a pull-down for the disk to display EPHC 4 - Create a pull-down for the disk to display EPHC
GP21_42	GP21_42_N	Plant Supervisor Control	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_43	GP21_43_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_44	GP21_44_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_45	GP21_45_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_81	GP21_81_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_82	GP21_82_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)
GP21_83	GP21_83_N	Global	209 PLS	1 - No User/Owner (Internal) 2 - No User/Owner (Internal) 3 - No User/Owner (Internal) 4 - No User/Owner (Internal)

Table 2-28. Hardware Straps (Sheet 2 of 3)

[illegible]

Table 2-28. Hardware Straps (Sheet 3 of 3)

GPID #	File Name	Purpose	Internal Terminations	File Usage/Description/Priority
GPID_282	OWM_BSL_RSP	RNDV	20K DP	Ensure that this string is pulled IOWM when BSLM, AZT, or security for normal position operation.
GPID_283	OWM_NIZ_2P	RNDV	20K DP	Ensure that this string is pulled when BSLM, AZT, or security for normal position operation.
GPID_284	OWM_NIZL_RSP	RNDV	20K DP	Ensure that this string is pulled IOWM when BSLM, AZT, or security for normal position operation.
GPID_285	OWM_NIZSET_N	RNDV	20K DP	Ensure that this string is pulled IOWM when BSLM, AZT, or security for normal position operation.
GPID_286	VTAL_LANE2P	RNDV	20K DP	Ensure that this string is pulled IOWM when BSLM, AZT, or security for normal position operation.

Table 5-3. Gemini Lake SoC Power Rail DC Specification and Iccmax


Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0V, 0.45-1.3	With AVP¹: DC Load Line (DCLL) = 6 mOhms Ripple at Iccmax = +/-15mV TOB ² _Iccmax = +/-20mV Overshoot voltage (max) = 100mV Overshoot duration (max) = 50 μ s	Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I2C VID are voltage control interface supported.	25
VNN_SVID	0V, 0.45-1.24	+/-5% at VID>1.0V; +/-50mV at VID<=1.0V	Variable voltage supply to other (non core) logic	5.6
VCCIOA	0V, 0.45-1.24	+/-5% at VID>1.0V; +/-50mV at VID<=1.0V	Notes: 1. Tie VCCIOA to VCCRAM_1P05 for DDR4 designs 2. Tie VCCIOA to VDDQ for LPDDR4 designs	-
VCCRAM_1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	2.7
VCCRAM_1P05_IO	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VDD2_1P2_GLM	1.2	+/-5%	Fixed voltage rail for SoC L2	2.5
VDD2_1P2_AUD_ISH			Fixed voltage rail for Audio and ISH I/O Logic	
VDD2_1P2_MPHY			Fixed voltage rail for MPHY Logic	
VDD2_1P2_USB2			Fixed voltage rail for USB2 I/O	
VDD2_1P2_DSI_CSI			Fixed voltage rail for MIPI* I/Os	
VDD2_1P2_PLL			Fixed voltage rail for PLLs	
VCC_1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic, and USB2 PHY	0.15
VDDQ	1.2 (DDR4)	+/-5%	Fixed voltage rail for DDR4 PHY	-
	1.1 (LPDDR4)		Fixed voltage rail for LPDDR4 PHY	3
VCCRTC_3P3V	2-3.47		Fixed Voltage rail for RTC (Real Time Clock)	-

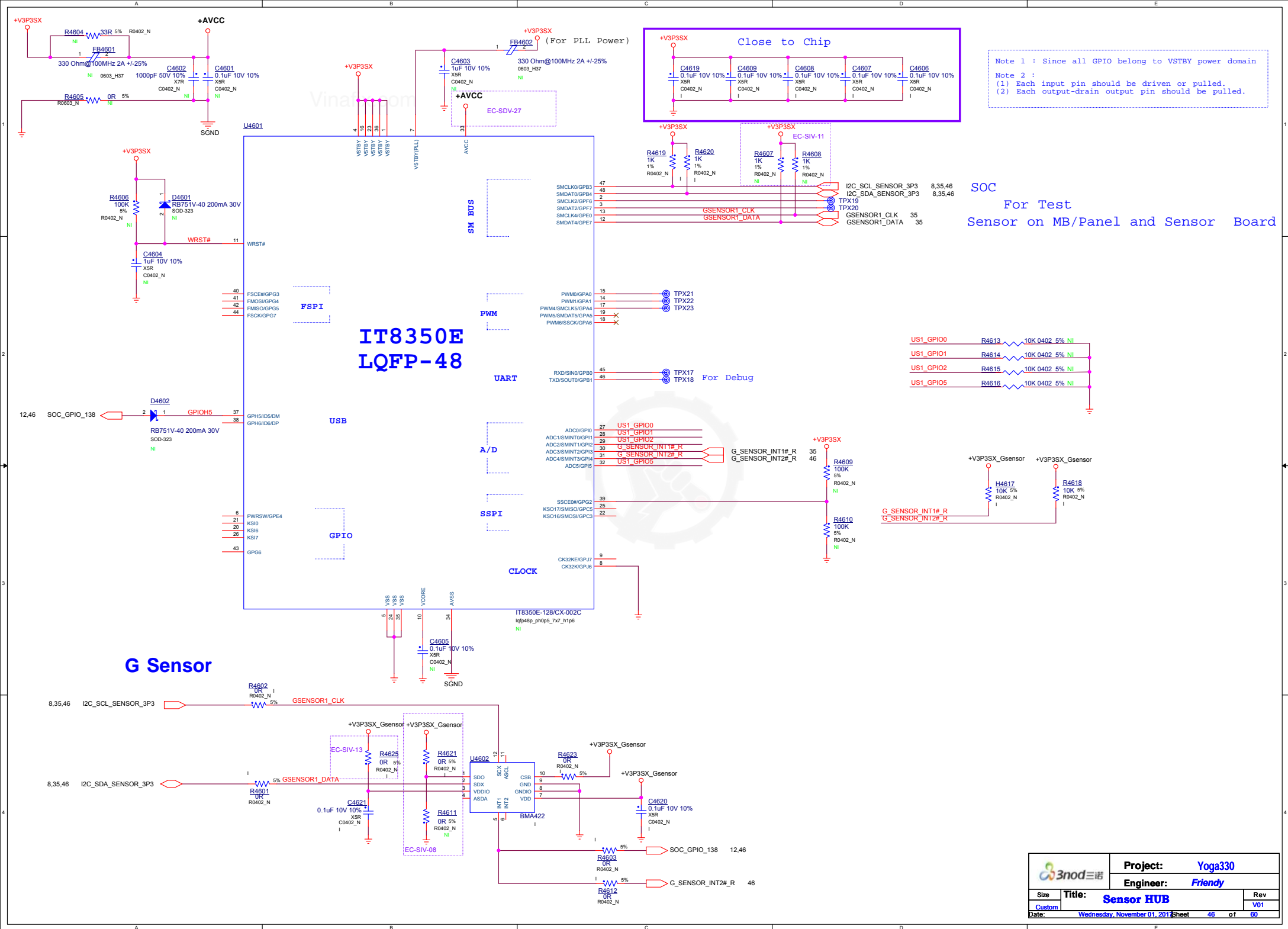
Notes:

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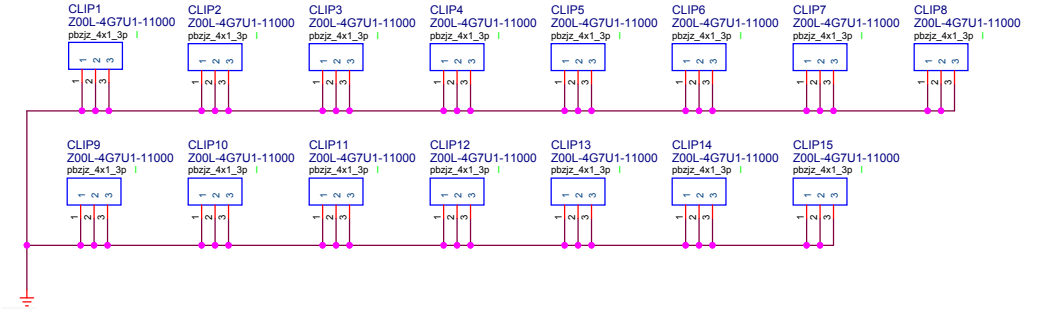
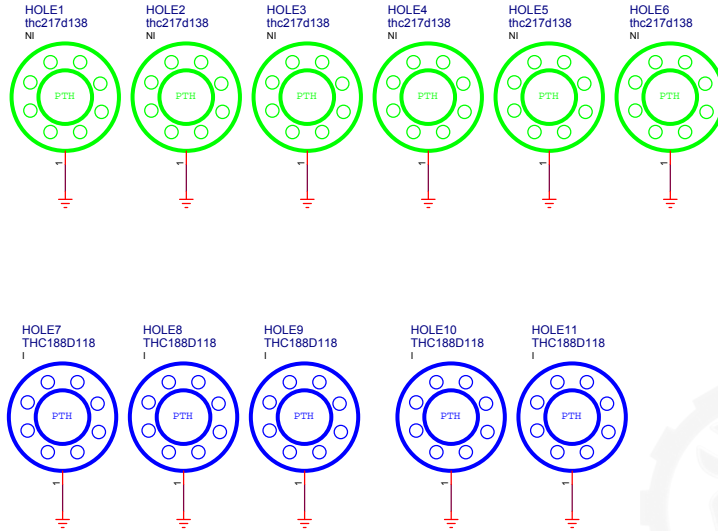
shy_x_mrd -
Wed Jun 03 11:22:42 2015

		Project: Yoga330	
		Engineer: Friendly	
Size	Title: CPU POWER	Rev	
Custom		V01	
Date: Wednesday, November 01, 2017		Sheet 45 of 60	



Shielding

Holes



INTERNAL ONLY

BPAGE DRAWING

shy_x_mrd_...
Wed Jun 03 11:22:42 2015

		Project: Yoga330	
Size		Engineer: Friendly	
Custom		Title: HOLE	
Date: Wednesday, November 01, 2017		Rev: V01	
Sheet 47 of 60			

EE Changelist


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INTERNAL ONLY

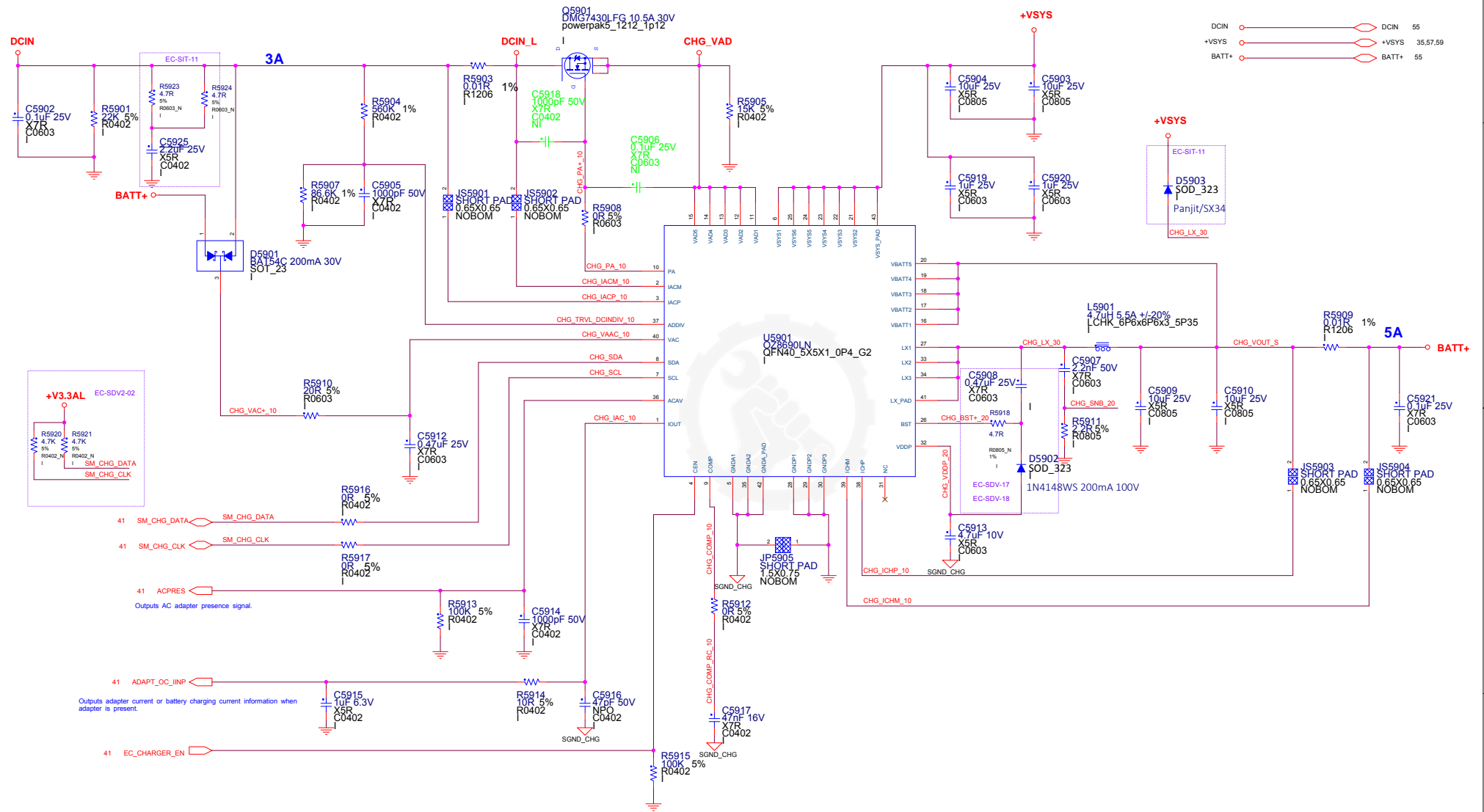
BPAGE DRAWING

shy_x_mrd -
Wed Jun 03 11:22:42 2015

		Project: Yoga330	
		Engineer: Friendly	
Size	Title: Changelist		Rev
Custom			V01
Date: Wednesday, November 01, 2017		Sheet 48 of 60	

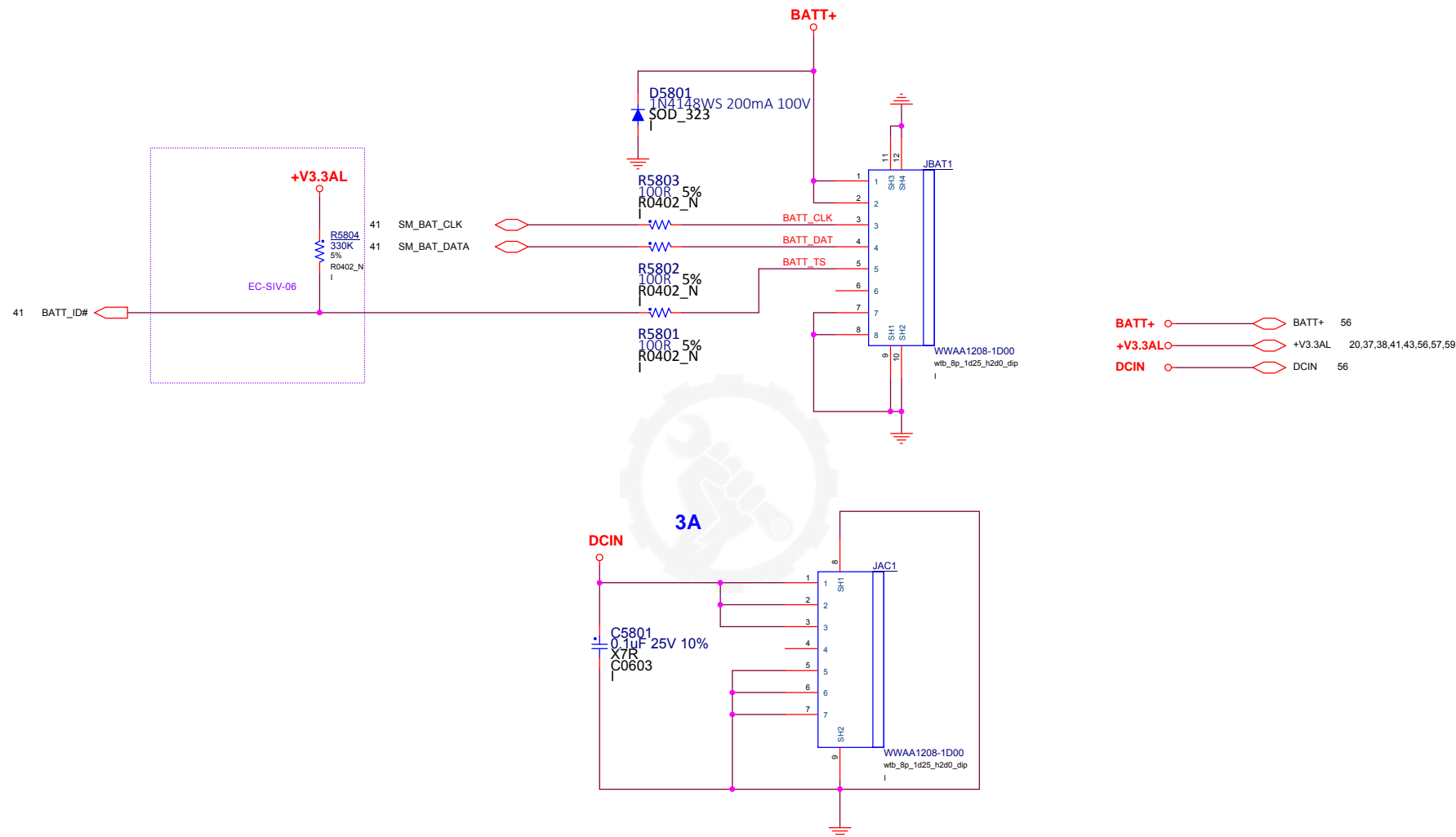
56: BATTERY CHARGER

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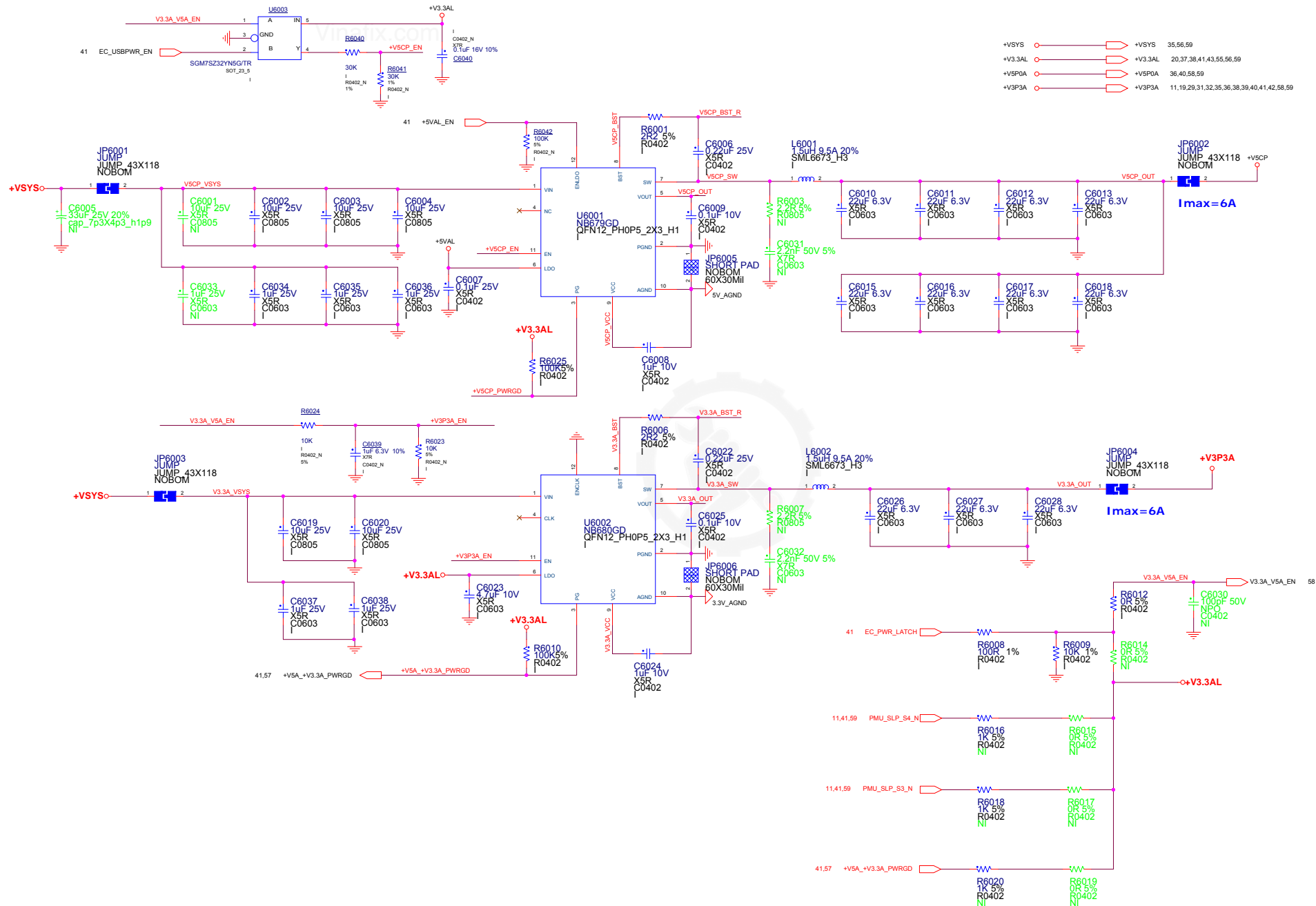
Project: Yoga330	
Engineer: Friendly	
Size: Custom	Title: Charger
Date: Wednesday, November 01, 2011	Rev: v01
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55: DC-IN & BATTERY CONNECTOR

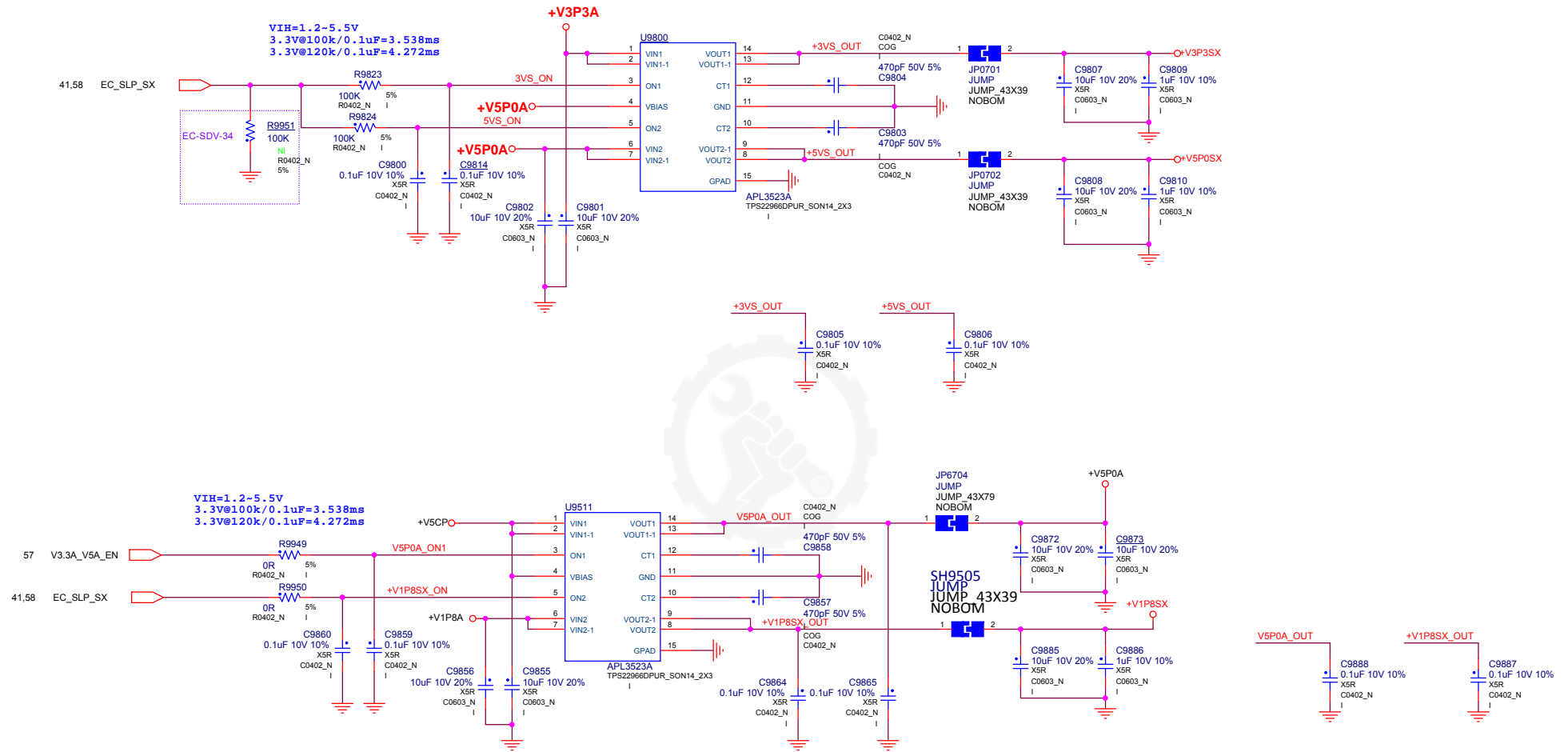


		Project:	Yoga330
		Engineer:	Friendly
Size	Title:	AC&Battery	
Custom		V01	
Date:	Wednesday, November 01, 2017	Sheet	55 of 60

57: +V5CP / +V3P3A POWER SUPPLY



58: +V5P0SX / +V3P3SX/ +V1P8SX/ +V5P0A POWER SUPPLY

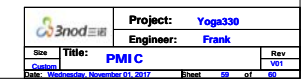


		Project: Yoga330	
		Engineer: Friendly	
Size	Title: 5V&3V	Rev	
Custom		V01	
Date:	Wednesday, November 01, 2017	Sheet	58 of 60

BPAGE DRAWING

INTERNAL ONLY

Rev: 0.0A
Fri May 27 06:47:28 2016



Power Map


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INTERNAL ONLY

BPAGE DRAWING

shy_x_mrd -
Wed Jun 03 11:22:42 2015

		Project: Yoga330	
		Engineer: Friendly	
Size	Title: Changelist		Rev
Custom			V01
Date: Wednesday, November 01, 2017		Sheet 60 of 60	